Automated High Throughput Optimization for Halide Perovskite Memristors

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1. Introduction

The rapid growth of artificial intelligence has exposed fundamental energy and bandwidth limits in von Neumann architectures, motivating the development of neuromorphic hardware that co-locates memory and computation. Memristors are a leading candidate for such systems due to their scalability and ability to mimic synaptic plasticity. Among material candidates, 2D halide perovskites (e.g., PEA_2PbBr_4) offer exceptional tunability and low-energy switching.[1], [2] However, optimizing these materials is hindered by a vast design space involving multiple processing parameters (e.g., concentration, solvent ratios, spin dynamics) and the inherent stochasticity of resistive switching mechanisms. Conventional manual optimization is too slow to navigate this complex landscape effectively, creating a critical bottleneck in deploying perovskite memristors for practical applications.

2. Methodology and Main Contribution

To address this challenge, we developed a fully automated high-throughput experimentation (HTE) workflow that integrates thin-film fabrication with autonomous electrical characterization. The system couples "SPINBOT," a custom automated spin-coating platform, with "ViPSA" (Vision-based Probing and Sensing Automation), enabling closed-loop synthesis and testing without human intervention.

Using this platform, we systematically explored the processing space of PEA_2PbBr_4 memristors, varying precursor concentration, spin speed, acceleration, and DMF:DMSO solvent ratios. This generated a large-scale statistical dataset spanning dozens of unique process conditions, revealing that processing conditions primarily modulate the statistical dispersion of switching metrics rather than just their mean values.

Building on this data, we implemented a multi-objective Bayesian optimization framework. Unlike standard grid searches, this machine learning approach actively directs the experimental loop to identify optimal processing windows that balance competing performance objectives—specifically, maximizing device yield while simultaneously maximizing the ON/OFF resistance ratio. This automated, AI-driven approach successfully identified robust processing conditions that mitigate stochastic variability, demonstrating a scalable pathway for accelerating the development of reliable neuromorphic hardware.

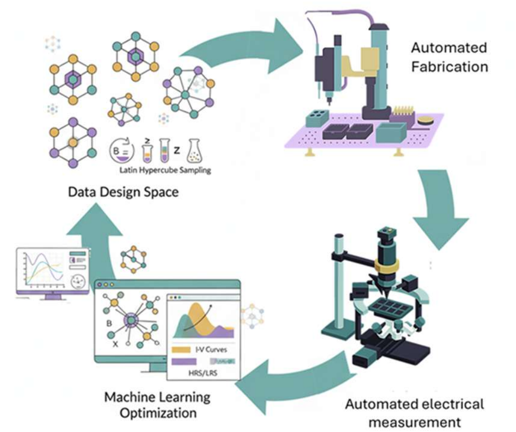

Fig. 1: Schematic representation of the workflow

Prior work on perovskite memristors has largely relied on manual trial-and-error or small-scale studies, often reporting "hero" devices that do not reflect statistical reality.[3], [4] While high-throughput methods have been applied to perovskite photovoltaics, their application to electrical characterization remains limited due to the complexity of contacting and testing large device arrays.[5] Our work advances the field by establishing one of the first fully automated electrical HTE workflows for memristors, capable of generating statistical datasets comparable to mature oxide-based RRAM technologies.

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References

[1] M. Ahmad, H. Kim, H. Patil, Y. H. Lee, and D. Kim, “2D and quasi-2D halide perovskite-based artificial synapses: highlights,” *J. Mater. Chem. C*, vol. 13, no. 36, pp. 18540–

18554, Sep. 2025, doi: 10.1039/D5TC00530B.

[2] M. An *et al.*, “Layered lead-free perovskite memristors with ultrahigh on/off ratio,” *Appl. Surf. Sci.*, vol. 701, p. 163317, Aug. 2025, doi: 10.1016/j.apsusc.2025.163317.

[3] D. Ielmini, S. Balatti, Z.-Q. Wang, and S. Ambrogio, “Variability and cycling endurance in nanoscale resistive switching memory,” in *2015 IEEE 15th International Conference on Nanotechnology (IEEE-NANO)*, Jul. 2015, pp. 124–127. doi: 10.1109/NANO.2015.7388864.

[4] M. Lanza *et al.*, “Standards for the Characterization of Endurance in Resistive Switching Devices,” *ACS Nano*, vol. 15, no. 11, pp. 17214–17231, Nov. 2021, doi: 10.1021/acsnano.1c06980.

[5] E. B. Miftahullatif *et al.*, “Machine-Learning-Driven in-Device Optimization of All-Printed Perovskite Solar Cells,” *ACS Energy Lett.*, vol. 10, no. 8, pp. 3952–3961, Aug. 2025, doi: 10.1021/acsenergylett.5c01475.