A Power-Efficient Analog Hardware Type-2 Fuzzy Classifier Architecture for Parkinson's Disease

Evangelos Asitzoglou, Daniela Papa,Vassilis Alimisis,
Andreas Papathanasiou, Vasileios Moustakas,
Evangelos Georgakilas and Paul P. Sotiriadis
Department of Electrical and Computer Engineering,
National Technical University of Athens, 15780 Athens, Greece
and Archimedes, Athena Research Center, Marousi, Greece.
E-mail: alimisisv@gmail.com

***Abstract*—Analog integrated fuzzy inference systems offer an energy-efficient hardware approach for biomedical classification tasks. This work presents an ultra-low-power fully analog hardware fuzzy classifier comprising Gaussian membership function circuits, a MIN/MAX-based rule evaluation stage, and an analog operational transcoductance amplifier as defuzzification block. The whole design improves robustness and current matching while maintaining low power consumption and delay. The Parkinson's disease dataset considered in this study is characterized by high dimensionality and strong feature correlations. To reduce hardware complexity and data overlap, the five most classification-relevant features are selected, enabling efficient hardware implementation while preserving classification performance. The proposed classifier is implemented in a TSMC 65 nm CMOS process and evaluated on the Parkinson's dataset. Post-layout simulation results demonstrate correct operation with a classification accuracy of 83.81% and a total power consumption of 138 nW, confirming its suitability for ultra-low-power biomedical edge applications.**

***Index Terms*—analog integrated design, power-efficient architecture, fuzzy classifier, Parkinson disease**

I. Introduction

Uncertain and imprecise data, such as those encountered in biomedical applications, tend to have measurement noise and variability across individuals, leading to overlapping feature distributions and unclear class boundaries [1]. In such conditions, hard computing techniques that rely on precise mathematical formulations often demonstrate unstable behavior and limited generalization performance [2]. These limitations have motivated the adoption of soft computing techniques that integrate fuzzy-based reasoning with compact neural network models, enabling hybrid intelligent systems capable of data-driven learning under uncertainty [3]. Within fuzzy logic, each input is associated with a degree of membership to the corresponding fuzzy set, allowing robust decision-making under poorly separated data [4].

Alongside these challenges, advances in Machine Learning (ML) and Artificial Intelligence (AI) have expanded the capabilities of data-driven modeling in biomedical applications [5]. Specifically, current research has increasingly focused on ML and AI models that can be trained offline and deployed locally with minimal energy and computational overhead [6], [7]. Offline training combined with local deployment enables training and parameter tuning to be performed off-device while maintaining energy-efficient and low-latency inference during operation [8], [9].

While fuzzy classifiers can be implemented in software or digital hardware [10], [11], such approaches usually exhibit non-negligible energy consumption and increased latency when continuous classification is performed in systems with limited resources, due to clocking, memory access and computational overhead. In contrast, analog implementations enable real-time inference with predictable latency and significantly reduced consumption, making them appropriate for continuous operation in resource-constrained systems.

Inspired by these developments, we present an ultra-low-power analog Type-2 Mamdani Fuzzy Inference System (FIS) applied to Oxford Parkinson's Disease Detection Dataset [12]. The proposed architecture processes weakly separated features by computing the Gaussian membership degrees, addresses a proper set of fuzzy "if-then" rules through MIN/MAX blocks, and converts the output into a binary decision utilizing a CMOS Operational Transconductance Amplifier (OTA).

Compared with previous works [13], [14], [15] this approach is intended as a complementary extension rather than a replacement. An enhanced version of the MIN/MAX circuit reported in [16] is presented, where cascode current mirrors are employed instead of the original bias current scheme, while preserving comparable accuracy, power consumption, and delay. Moreover, the Parkinson's dataset is challenging to process, as it consists of 22 features, and the selection of the most impactful ones depends on their relationship with the final prediction. In this work, the 5 most classification-relevant features are selected in order to reduce the data overlap and the complexity while maintaining high accuracy, both in software and hardware implementations.

The paper proceeds as follows: Section II provides background on fuzzy logic fundamentals. Section III presents the proposed analog fuzzy classifier architecture. Section IV describes the offline training procedure and the resulting architecture tunability. Section V reports simulation results and biomedical data analysis. Section VI provides a comparison with related works and discusses the obtained results. Section VII, concludes the paper.

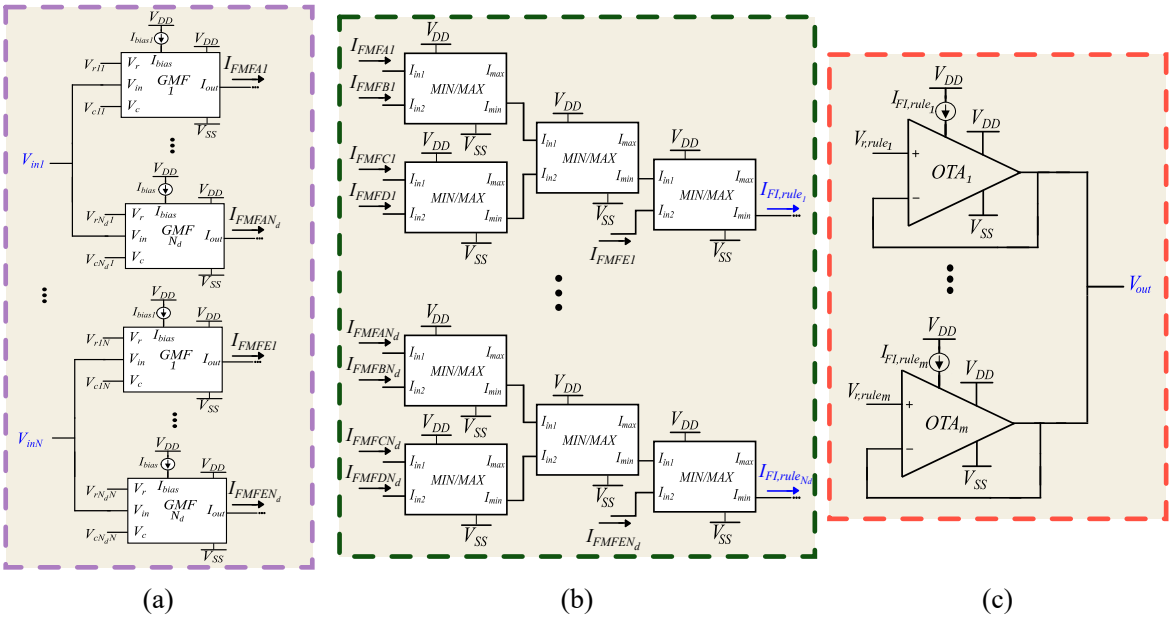


Fig. 1: High-level architecture of the proposed FIS. (a) Fuzzification block. (b) Rule evaluation stage. (c) COG implementation.

II. Background

Fuzzy systems are a key part of soft computing and are designed to handle uncertain or vague information while producing comprehensible results [17]. They are based on fuzzy set theory [18] where elements are assigned degrees of membership unlike classical set theory where elements either belong or do not to a set. Fuzzy reasoning provides a mechanism for combining these variables through a process also known as generalized modus ponens (GMP). Similar to human reasoning, where conclusions are drawn qualitatively from concepts, fuzzy systems use if-then rules, with the antecedent and consequent part represented as fuzzy sets [19]. An example of a if-then rule is illustrated as follows:

- Ant 1: x is A'
- Ant 2: if x is A, then y is B
- Conclusion: y is B'

where typically A, A', B, and B' are fuzzy sets.

Fuzzy Inference Systems (FIS) implement fuzzy reasoning in practice and typically consist of four main blocks [20]. The first block is fuzzification, where crisp inputs are converted into fuzzy sets, using Membership Functions (MFs). Various types of MFs are commonly used in the literature including Gaussian, Triangular, Trapezoid functions and others. In the second block, the fuzzified inputs are applied to the Rule Base and then evaluated by the Decision Unit to produce the fuzzified outputs. Different approaches to rule evaluation have led to well-known fuzzy inference models, such as Mamdani, Takagi-Sugeno and Tsukamoto [21]. Finally, in the Defuzzification block the fuzzy outputs are transformed into crisp values, suitable for real-world applications. Several methods exist for defuzzification, including the Center of Gravity (COG), Middle of Maxima (MOM), and the Max criterion among others [22].

Moreover, FIS provide a versatile architecture in which each component can be adapted to suit the requirements of a specific application. As a result, they are widely used in various fields including robotics, control systems, image processing, neurofuzzy systems and medical applications [23]–[26]. The rising demand for real-time, low power applications has prompted a shift toward hardware implementations of FIS. While digital solutions such as FPGA based designs offer high computational performance ,they fail to meet low power requirements in energy constrained applications [27]. As a result analog implementations, specifically circuits operating in subthreshold regime, offer reduced power consumption [13]. Furthermore, Analog FIS are advantageous for biomedical applications where continuous-time signals require real-time processing and low power consumption.

III. Proposed Architecture

In this section the implementation of the proposed analog FIS will be discussed. Its operation is described through three main subsections, the fuzzification, rule evaluation and defuzzification. All circuits operate in subthreshold region, with supply rails of $V_{DD} = -V_{SS} = 0.3V$ and are designed in the TSMC 65nm CMOS process.

A. Fuzzification Block

In the fuzzification stage the input voltage is converted to a fuzzy input representing its degree of membership to each corresponding fuzzy set. In this work Gaussian Membership Functions are employed. The use of Gaussian MF is beneficial for representing uncertainty in measurements. The smoothness and symmetry of the Gaussian Function allows representing each input effectively. Furthermore, the gaussian parameters, center and width, can be adjusted easily to reflect the input data characteristics [28].

The circuit used in this architecture to generate the Gaussian Functions is a modified Bump circuit as illustrated in Fig. 2. This modified bump [29] combines a linearization technique within the basic building blocks of Delbruck's Bump [30], to produce a more precise Gaussian function with parameters that can be adjusted electronically, V_r sets the center, V_c controls the width and I_{bias} determines the amplitude, as shown in Fig. 3. The transistors dimensions of the Gaussian MF are given in Table I. During fuzzification process, the voltage input V_{in}, associated with a linguistic term, is applied to the corresponding Gaussian MF and the produced output current encodes the degree of membership,as illustrated in Fig. 1. This current signal is subsequently used as an input to the following stage, the rule evaluation.

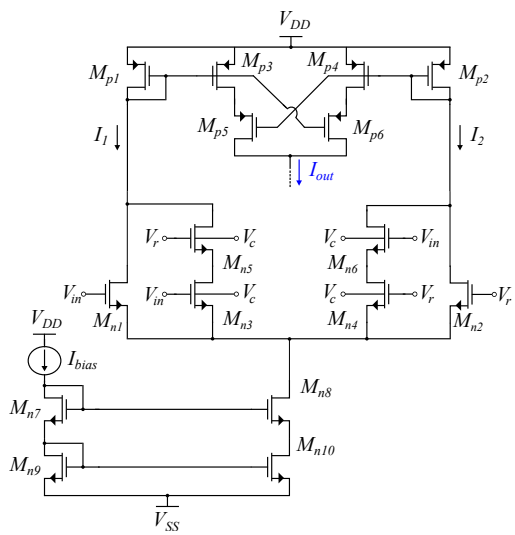


Fig. 2: Gaussian Function Circuit (All bulk connections not explicitly shown are assumed to be connected to V_{DD} for PMOS and V_{SS} for NMOS transistors)

TABLE I: Dimensions of MOS Transistors in Gaussian MF

Differential pair	W/L(μm/μm)	Current correlator	W/L(μm/μm)
M_{n1},M_{n2}	2.0/0.8	M_{p1},M_{p2}	1.2/1.2
M_{n3},M_{n4}	0.8/2.0	M_{p3}-M_{p6}	2.4/1.2
M_{n5},M_{n6}	1.0/2.0	-	-
M_{n7},M_{n9}	3.2/1.5	-	-
M_{n8},M_{n10}	2.4/1.5	-	-

B. Rule Evaluation

At this stage, each rule is evaluated by computing its firing strength from the input membership degrees obtained in the previous stage. Logical AND/OR operations are implemented through MIN/MAX blocks, and the resulting rule outputs are aggregated to form the final output fuzzy set. The proposed MIN/MAX circuit, shown in Fig. 4, is derived from the architecture reported in [16], with the bias current sources of the second input replaced by cascode current mirrors, resulting in reduced power consumption. The circuit compares two competing input currents, I_1 and I_2, using a PMOS cross-coupled pair. When $I_1 > I_2$, the cross-coupled structure forces

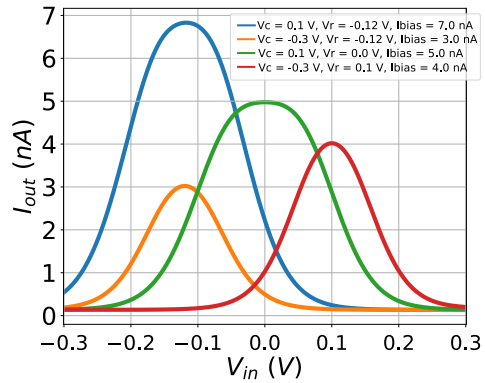


Fig. 3: Output current I_{out} for various values of V_c, V_r and I_{bias}.

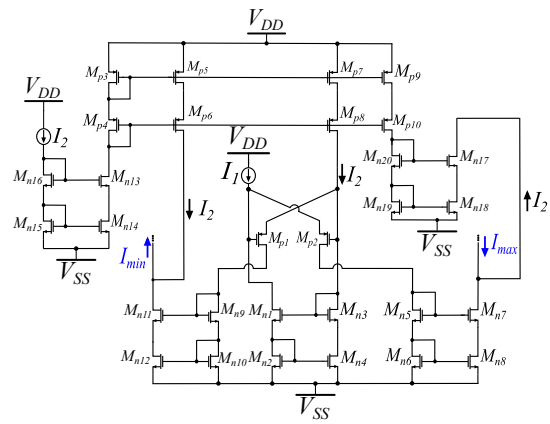


Fig. 4: Proposed MIN/MAX circuit implementation used for fuzzy rule evaluation.

one PMOS transistor into cutoff while the other remains active, generating a differential current

$$I_\Delta = I_1 - I_2. \tag{1}$$

An adapted Wilson current mirror enforces equal current flow in the input branches and mirrors I_Δ to the MAX output node. By applying Kirchhoff's current law at the MAX node, the resulting output current is

$$I_{\max} = I_2 + (I_1 - I_2) = I_1. \tag{2}$$

At the same time, the current at the MIN output node is

$$I_{\min} = I_2, \tag{3}$$

since the corresponding branch carries zero differential current. The same operation applies symmetrically when $I_1 < I_2$, yielding

$$I_{\max} = \max(I_1, I_2), \qquad I_{\min} = \min(I_1, I_2). \tag{4}$$

The circuit's results in sinusoidal inputs are shown in Fig. 5 and Fig. 6 while the CMOS transistor dimensions are summarized in Table II.

Based on the offline training process applied to the Parkinson's disease dataset, it was shown that the rules in which the

classifier provided robust behavior and better accuracy were the following:

$$I_{\rho_0} = \min\{I_{\text{FMFA0}}, I_{\text{FMFB0}}, I_{\text{FMFC0}}, I_{\text{FMFD0}}, I_{\text{FMFE0}}\} \tag{5}$$

$$\text{I}_{\rho_1} = \min\{I_{\text{FMFA1}}, I_{\text{FMFB1}}, I_{\text{FMFC1}}, I_{\text{FMFD1}}, I_{\text{FMFE1}}\}$$

where $I_{\text{FMF}A_i}$ denotes the output of the membership function corresponding to feature A and class i.

However, for a general purpose classification, both MIN and MAX operators are crucial.

TABLE II: Dimensions of MOS Transistors in the MIN/MAX Circuit

Device	W/L (μm/μm)	Device	W/L (μm/μm)
M_{n1}–M_{n4}	4.0/0.3	M_{p1},M_{p2}	4.0/0.6
M_{n5}–M_{n8}	3.2/0.6	M_{p3}–M_{p10}	6.0/0.24
M_{n9}–M_{n12}	4.0/0.6	–	–
M_{n13}–M_{n20}	8.0/1.2	–	–

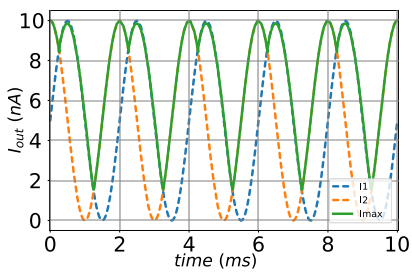


Fig. 5: Transient Analysis of Maximum output current I_{max}

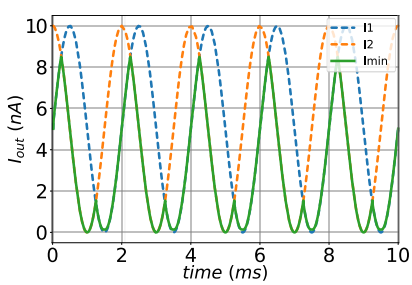


Fig. 6: Transient Analysis of Minimum output current I_{min}

C. Defuzzification Block

The method chosen for defuzzification is Center of Gravity (COG), where the output currents from the previous stage, fuzzy inference, are transformed into crisp outputs. The COG method calculates the center of area defined by the fuzzy output set, and uses this value as the defuzzified output. If C represents a fuzzy output set, then according to COG [19] the defuzzified output is computed as:

$$z_0 = \frac{\int_a^b zC(z)\,dz}{\int_a^b C(z)\,dz} \tag{6}$$

Following the methodology in this work [13] the final expression for the COG output is given by:

$$COG = \frac{\sum_{i=1}^{m} w_i c_i}{\sum_{i=1}^{m} w_i} \tag{7}$$

where w_i is the firing strength of the rule i, c_i is the centroid of the corresponding MF and m is the total number of rules. In this implementation, the firing strength of rule i is given by the fuzzy inference output current $I_{fi,rule_i}$ and the centroid of the Gaussian MF is represented by the reference voltage $V_{r,rule_i}$, as a result the final expression is:

$$COG = \frac{\sum_{i=1}^{m} I_{fi,rule_i} V_{r,rule_i}}{\sum_{i=1}^{m} I_{fi,rule_i}} \tag{8}$$

To realize this equation at circuit level, the adopted approach employs a total of m Operational Transconductance Amplifiers (OTAs), connected in a feedback configuration, utilizing the voltage follower-aggregation technique [31], as illustrated in Fig. 1. The corresponding circuit analysis is based on the methodology presented in [13].

The implemented OTA, shown in Fig. 7, incorporates a symmetric source degeneration in the differential input pair, enhancing linearity. The bias current of the OTA is derived from the rule evaluation $I_{fi,rule_i}$ and the non-inverting input V_+ receives the $V_{r,rule_i}$ from the corresponding output Gaussian MF. In this design symmetric source degeneration was chosen to linearize the differential pair M_{n1} and M_{n2} while achieving higher transconductance (G_m) values, contributing to more accurate computation of the COG. The G_m values over the differential input ΔV_{in} are demonstrated in Fig. 8a and the output current I_{out} across ΔV_{in} presenting a clear linear range of at least 200mV, shown in Fig. 8b. Additionally, the final output is a voltage, eliminating the need for analog-to-digital or current-to-voltage conversion circuits. The circuit's transistor dimensions are given in Table III.

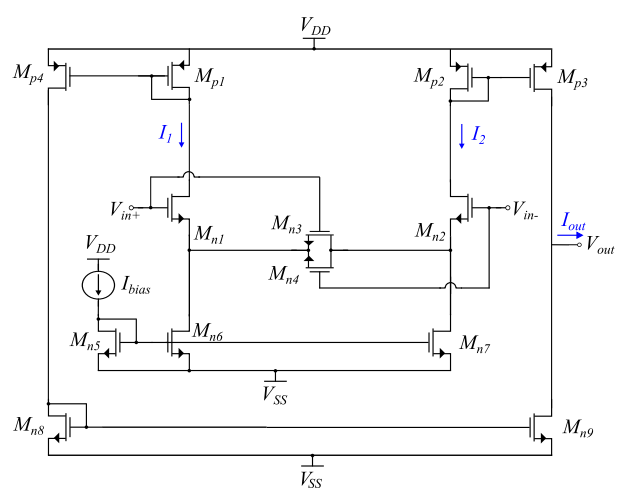
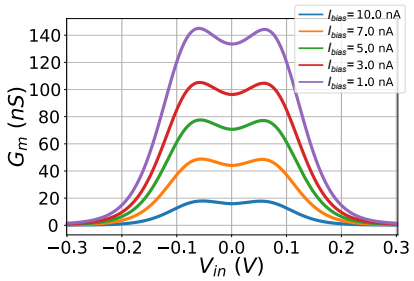


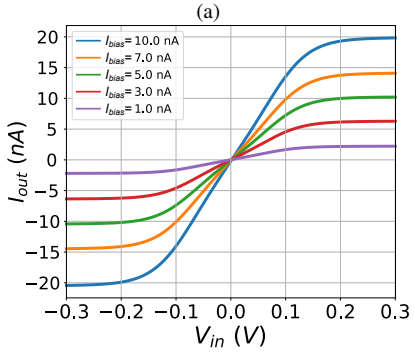
Fig. 7: Operational Transconductance Amplifier (OTA), used for the Defuzzification block.

TABLE III: Dimensions of MOS Transistors in OTA

Differential pair	W/L(μm/μm)	Current mirrors	W/L(μm/μm)
M_{n1},M_{n2}	6.4/12.0	M_{p1},M_{p4}	0.8/12.0
M_{n3},M_{n4}	0.8/12.0	M_{p2},M_{p3}	0.8/12.0
M_{n5}-M_{n7}	0.2/12.0	M_{n8},M_{n9}	0.2/12.0



(a)



(b)

Fig. 8: (a) Transconductance (G_m) values of the OTA across ΔV_{in}. (b) Current output I_{out} of the OTA across ΔV_{in}.

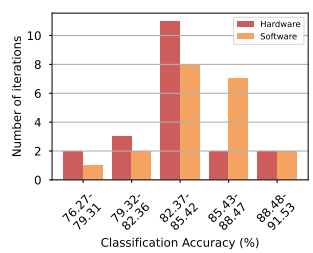
IV. Offline Training and Architecture Tunability

The proposed architecture is fully programmable through modification of the characteristics of the Gaussian MFs. These adjustments are implemented offline in software where the data handling, training and evaluation are carried out. Specifically, altering the appropriate control signals representing voltages V_r, V_c, and current I_{bias}, results in the tuning of mean value, variance, and amplitude of the MFs. Hence, if data change or are added, the software is able to modify the shape of the Gaussian fuzzy sets accordingly and in cooperation with hardware, the classification remains consistent. During the offline training phase, the rule base as well as the Gaussian parameters are defined and optimized in software in order to be compatible with the hardware implementation. The input data is normalized to comply with the operating range of the analog blocks and the rules are formulated by pre-proccesing the statistical structure of data features utilizing a software-based system. As mentioned in previous sections, each input and output MF corresponds to a Gaussian circuit in the fuzzification stage and an OTA-diffusor circuit in the defuzzification stage, respectively. Consequently, any MF which is not needed can be deactivated by disabling the bias current of its corresponding circuit, reducing the overall power consumption, leading to enhanced architectural flexibility.

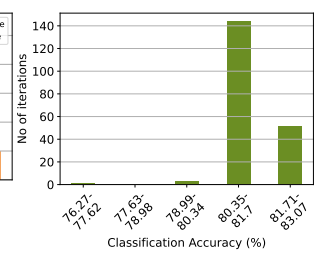
V. Simulation Results and Data Analysis

In this section, we present the application utilized to assess the performance of the proposed analog fuzzy classifier, along with the corresponding simulation results. The dataset used in this application is a publicly available biomedical dataset on Parkinson's disease, which can be accessed via the UCI Machine Learning Repository [12]. The dataset includes 195 voice recordings from 31 people, 23 of whom are diagnosed with Parkinson's disease. The objective of the dataset is to distinguish healthy people and those with Parkinson's disease by using the binary status label. It consists of 22 continuous numeric features, as a result in order to reduce complexity 5 features were chosen that demonstrated the highest relevance in classification. The selection was based on Principal Component Analysis (PCA), identifying the features that contributed the most [32]. Further details about the dataset are available here [33].

Post-layout simulations of the fuzzy classifier were implemented using the TSMC 65nm CMOS process via Cadence Virtuoso. The layout of the classifier is presented in Fig. 10, occupying an area of $91\,\mu\text{m} \times 284\,\mu\text{m}$. A series of evaluation tests were conducted to account for random effects, including training over 20 iterations and a Monte Carlo simulation. The results are presented in Fig. 9a for the 20 iterations and in Fig. 9b for the Monte Carlo simulation with $N = 200$ points. As observed in Fig. 9a the proposed fuzzy classifier achieves accuracies between 76.27% and 89.83% with an average accuracy of 83.82%. For comparison, a software-based model was implemented, that reaches an accuracy of 91.53%, demonstrating that the classifier provides comparable performance. The robustness of the proposed classifier was further evaluated through Monte Carlo simulation, as shown in Fig. 9b, where the classification accuracy ranges from 76.27% and 83.05%, with an average of 81.75% and a standard deviation of 0.87%, indicating stable performance under random variations.



(a)



(b)

Fig. 9: (a) Accuracy of the Software and Hardware implementations for 20 iterations. (b) Monte Carlo simulation of the proposed architecture with $N = 200$ points.

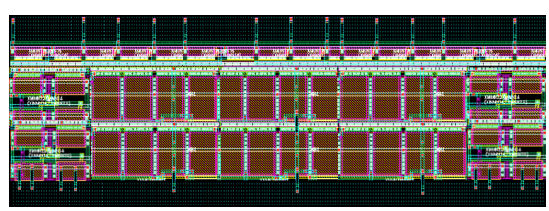


Fig. 10: Layout of the proposed FIS architecture, its dimensions are $91\,\mu\text{m} \times 284\,\mu\text{m}$

TABLE IV: Comparison of analog classifiers on the classification dataset.

	Classifier	Worst accuracy	Median accuracy	Max accuracy	Power consumption	Classification speed	Energy per classification	Complexity
This work	Fuzzy	76.27%	83.81%	89.83%	$138nW$	$10K\,\frac{\text{classifications}}{\text{s}}$	$\frac{13.8\text{ pJ}}{\text{classification}}$	Low
[34]	MLP	81.32%	87.56%	92.45%	$398.57\mu W$	$820K\,\frac{\text{classifications}}{\text{s}}$	$\frac{486.06\text{ pJ}}{\text{classification}}$	High
[35]	LSTM	91.40%	95.23%	98.41%	$41.38mW$	$870M\,\frac{\text{classifications}}{\text{s}}$	$\frac{47.56\text{ pJ}}{\text{classification}}$	High
[36]	RBF	75.17%	81.29%	88.34%	$53.28\mu W$	$200K\,\frac{\text{classifications}}{\text{s}}$	$\frac{266.4\text{ pJ}}{\text{classification}}$	Medium
[37]	ANN	77.60%	84.19%	88.60%	$4.97\mu W$	$3M\,\frac{\text{classifications}}{\text{s}}$	$\frac{1.66\text{ pJ}}{\text{classification}}$	Medium
[38]	K-means	81.50%	87.23%	93.60%	$156.18\mu W$	$5M\,\frac{\text{classifications}}{\text{s}}$	$\frac{31.24\text{ pJ}}{\text{classification}}$	High
[39]	Decision Tree	75.37%	81.69%	87.17%	$639\ nW$	$250K\,\frac{\text{classifications}}{\text{s}}$	$\frac{2.56\text{ pJ}}{\text{classification}}$	Medium
[40]	LVQ	75.98%	83.76%	88.67%	$325nW$	$100K\,\frac{\text{classifications}}{\text{s}}$	$\frac{3.25\text{ pJ}}{\text{classification}}$	Low
[41]	Voting	73.66%	79.48%	83.77%	$463nW$	$100K\,\frac{\text{classifications}}{\text{s}}$	$\frac{4.63\text{ pJ}}{\text{classification}}$	Low
[42]	ANN	79.64%	85.78%	93.44%	$5.18\mu W$	$650K\,\frac{\text{classifications}}{\text{s}}$	$\frac{7.96\text{ pJ}}{\text{classification}}$	Medium
[13]	Fuzzy	75.96%	82.95%	88.78%	$883nW$	$4.55K\,\frac{\text{classifications}}{\text{s}}$	$\frac{194.07\text{ pJ}}{\text{classification}}$	Medium
[43]	SVDD	80.37%	86.51%	90.22%	$61.3\ \mu W$	$530K\,\frac{\text{classifications}}{\text{s}}$	$\frac{115.66\text{ pJ}}{\text{classification}}$	Medium
[44]	SVR	81.22%	86.78%	92.47%	$92.3\ \mu W$	$870K\,\frac{\text{classifications}}{\text{s}}$	$\frac{106.09\text{ pJ}}{\text{classification}}$	Low
[45]	SVM	78.56%	82.36%	91.32%	$955.4\ \mu W$	$870K\,\frac{\text{classifications}}{\text{s}}$	$\frac{1098.16\text{ pJ}}{\text{classification}}$	High

VI. Comparison and Discussion

This work aims to establish a balanced optimization among power consumption, classification performance, and inference latency. As summarized in Table IV, the proposed design achieves the lowest power consumption among all compared implementations, while maintaining competitive classification accuracy and reduced energy per classification event. This highlights its superior energy efficiency compared to previously reported designs. All circuits were implemented in TSMC 65 nm CMOS technology and validated using the same dataset to ensure a uniform and objective benchmarking environment. Within this framework, the proposed architecture demonstrates an optimal trade-off between structural simplicity and predictive capability. Although increasing the model's complexity could further enhance classification performance, such improvements would inevitably lead to higher power dissipation and increased energy overhead. Thanks to its ultra-low power operation and compact architecture, the proposed design is particularly well suited for deployment as a wake-up circuit in energy-constrained systems. Its minimal power consumption enables continuous monitoring functionality, activating higher-power processing stages only when necessary. Therefore, the architecture represents an excellent candidate for use as an analog front-end classifier in high-precision analog and mixed-signal machine learning systems, especially in always-on and battery-powered applications.

VII. Conclusion

An ultra-low-power fully analog fuzzy classifier for biomedical applications was presented. The design combined Gaussian membership circuits, a MIN/MAX-based rule evaluation stage, and an OTA for defuzzification, achieving improved robustness, current matching, and minimal power consumption. The Parkinson's disease dataset was efficiently handled by selecting the five most relevant features, reducing hardware complexity while maintaining classification performance. Implemented in a TSMC 65-nm CMOS process, the classifier achieved 83.81% accuracy with 138 nW power consumption, demonstrating its suitability for low-power edge-AI biomedical monitoring.

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