A Tunable Energy-Efficient DPI-Based Leaky Integrate-and-Fire Neuron for Neuromorphic Applications

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***Abstract*—A low-power analog implemented DPI-based neuron is proposed in this paper. The design was carried out using TSMC's $65nm$ CMOS process node, targeting energy-efficient spiking with multi-parameter tunability. The proposed neuron combines a subthreshold differential pair integrator (DPI) membrane for tunable integration and logarithmic membrane dynamics with a modified $1N3P$ Schmitt trigger that reduces leakage to preserve its efficiency for low-power applications. Additionally, a current starved inverter provides independent control of spike width and refractory duration via a dedicated refractory/reset circuit. Operating from a 0.8 V power supply, the circuit simulations demonstrate a stable leaky integrate-and-fire behavior and controllable firing rates, consuming just $20.42fJ/spike$ at $51.5kHz$ spike frequency. These results suggest that the proposed neuron is a well suited building block for large-scale neuromorphic systems requiring robust low-power spiking and flexible parameter programmability.**

***Index Terms*—Low power, Neuromorphic circuit design, Analog Neuron Cell, Hysteresis, Neuron Tunability**

I. Introduction

Neuromorphic computing aims to reproduce the operation of biological neural systems using energy-efficient hardware [1], [2]. A key building block in such systems is the neuron circuit, which integrates synaptic currents and generates spikes. However, many conventional analog neuron designs suffer from high power consumption, especially during the membrane charging phase. This problem becomes more severe during high frequency operation, when rapid and repeated charging of the membrane is required. In addition, linear membrane dynamics commonly used in hardware neurons fail to capture the nonlinear behavior observed in biological neurons.

Leaky Integrate-and-Fire neurons embody the basic nonlinear functionality of biological neurons, while maintaining low circuit complexity [3], [4]. This type of silicon neuron is chosen here, against more biologically-plausible designs such as Hodgkin–Huxley [5], Izhikevich [6] and Resonate-and-Fire [7] neurons, which increase hardware complexity dramatically, but also against more simplistic Integrate-Fire neurons [8], which do not possess the required dynamics.

To address these limitations, this work presents a new neuron architecture based on DPI [1], [9]. The proposed DPI-based neuron significantly reduces power consumption during membrane charging by operating in the subthreshold regime, while naturally introducing a logarithmic membrane response. This logarithmic behavior closely resembles the dynamics of biological neurons and improves robustness without increasing circuit complexity. Importantly, these benefits are achieved without sacrificing performance or tunability, allowing the neuron to operate across a wide range of firing rates and time constants.

The proposed neuron is fully tunable and supports independent control of key parameters, such as membrane time constant, refractory period, and spike width. This flexibility enables more accurate implementations of neuromorphic algorithms in hardware, effectively increasing the network's weight resolution. As a result, the neuron is well suited for low-power neuromorphic systems that rely on event-driven processing, and can be seamlessly integrated across a wide range of network architectures and topologies.

The proposed architecture is implemented and evaluated using the Cadence IC design environment in a TSMC 65 nm CMOS process. Simulation results show that the proposed DPI-based neuron achieves low power consumption, stable logarithmic membrane behavior, and broad tunability range. All in all, the architecture supports energy-efficient spike generation while maintaining high tunability and performance. The proposed neuron stands as a trade-off between very-low power simplistic solutions [10], [11] and more complex, but power-hungry designs [2], [12].

The main contributions of this work are as follows: A novel DPI-based neuron architecture that reduces power consumption during membrane charging. A logarithmic membrane response that closely matches biological neuron behavior. Full tunability without performance degradation, enabling spike operation at various frequencies.

The remainder of this paper is organized as follows. Section II presents the proposed circuit architecture of the modified neuron cell. Section III reports simulation results and perfor-

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mance evaluation. In Section IV the performance comparison is provided. Finally, Section V concludes the paper.

II. Proposed Circuit Architecture

This section presents the architecture of a DPI-based neuron and explores its operation. This design aims to reduce the high power consumption during the charging phase of the membrane, while introducing logarithmic behavior, that resembles biological neurons, without sacrificing performance or tunability.

The design of the modified neuron, based on [13], is shown in Fig. 1. It consists of four sub-circuits. The DPI, the altered 1N3P Schmitt trigger, a current-starved inverter that enables the control of the width of the output spike and a reset and refractory control circuit. The operation of the neuron is extensively analyzed in the following.

The DPI divides the input current accumulated from previous neurons between M_{p2} and M_{p3}, depending on the value of V_{thr}. The current charging the membrane is determined by the dynamics of the differential pair, approximating a first-order low-pass filter with tunable time constant (through V_{lk}) and tunable gain (through V_{thr}), as explained in [1], [9]. Thus, both V_{lk} and V_{thr} can tune the DPI filter's response, and ultimately affect the output spiking frequency. The transistor M_{n1} also works as the leakage conductance, slowly discharging the membrane in the absence of input current. The inclusion of the DPI enables the use of the circuit in lower frequencies, which leads to the efficient process of real-world events and the natural synchronization with those signals [1].

The hysteresis comparator used is a modified version of a typical Schmitt trigger [14], [15], using only 1 NMOS (M_{n3}) and 3 PMOS (M_{p4}-M_{p6}) transistors (1N3P). It compares the input voltage from the DPI block to two distinct thresholds, one for the rising edge and one for the falling edge. To further separate the two thresholds, a high voltage threshold NMOS has been used for the transistor M_{n3}. When the membrane voltage exceeds the rising threshold, the comparator generates a low signal equal to V_{SS} and similarly, when the membrane falls below the lower threshold, it returns to a high signal equal to V_{DD}. The removal of the two NMOS transistors eliminates a direct leakage path from V_{DD} to V_{SS}, which caused high power consumption for the duration of the membrane charging. The PMOS path from V_{SS} to V_{DD} does not present such problems, due to the reset of the membrane being almost instantaneous. Therefore, the 1N3P Schmitt Trigger in this design results in a substantial decrease in power consumption while also maintaining an acceptable amount of hysteresis for a stable signal, despite membrane voltage fluctuations and noise. An analytical study of the conventional and the 1N3P Schmitt Trigger, can be found in [14], [15]. The output finally passes through an inverter in order to produce a clean positive output spike.

The current-starved inverter uses the output spike as its input, in order to have an adjustable delay of the signal, thus leading to a controllable pulse width. The spike goes through a CMOS inverter (M_{n11} and M_{p13}) that has its current limited through transistors M_{n10}, M_{n12}, M_{n13}, M_{p14} and M_{p15}, and is controlled by the bias voltage V_w. Restricting the current leads to a delayed spike that propagates through the inverter consisting of M_{n9} and M_{p12}. The membrane reset is thus delayed and the pulse width is effectively tuned by V_w. This control enables the circuit to implement multiple temporal coding strategies, such as rate coding, time to first spike and burst coding.

Lastly, the output of the current-starved inverter is routed, through the inverter consisting of M_{n9} and M_{p12}, to the Refractory and Reset part of the circuit. It consists of the transistor M_{n5}-M_{n8} and M_{p8}-M_{p11} and the capacitor C_r. A spike output from the current-starved inverter, turns M_{n8} on, which then discharges the capacitor C_r. The capacitor is then gradually charged again through M_{p11}, controlled by the bias voltage V_{rfp}, which decides the duration of the refractory period. When the voltage of C_r drops to V_{SS}, it raises the voltage V_{rf} to V_{DD}, through the chain of inverters (M_{n5}-M_{n7} and M_{p8}-M_{p10}), switching transistor M_{n2} on, which resets the membrane. The transistor M_{p1} is also switched off, in order to prevent the input current from charging the membrane during the refractory period. The tunable refractory period improves stability and energy efficiency by preventing excessive spiking while supporting additional learning behaviors and coding schemes.

The resulting circuit is highly adjustable over the key neuron parameters, such as refractory period, leakage rate and spike width, resulting in wide control over the output spikes characteristics. This enables its use in a wide range of operating conditions.

III. Simulation Results

The proposed neuron architecture was designed in the 65nm CMOS process using Cadence Virtuoso. The transistor dimensions of Fig. 1 are $\left(\frac{W}{L}\right)_n = \frac{200\text{nm}}{200\text{nm}}$ for NMOS transistors and $\left(\frac{W}{L}\right)_p = \frac{300\text{nm}}{200\text{nm}}$ for PMOS transistors, except for M_{n9}, M_{n11}, M_{p12} and M_{p13} which have $\left(\frac{W}{L}\right) = \frac{500\text{nm}}{200\text{nm}}$, while M_{n8} has $\left(\frac{W}{L}\right) = \frac{200\text{nm}}{500\text{nm}}$. The membrane capacitor has $C_{mem} = 400fF$, while the refractory capacitor has $C_r = 100fF$. Finally, the voltage supply rails for the neuron are $V_{DD} = 0.8V$ and $V_{SS} = 0V$, enabling subthreshold operation for the DPI block and sustaining very low power consumption for the whole neuron.

In Fig. 2 the output spikes of the neuron V_{spike} are shown for a constant input current I_{in}, i.e. prolonged depolarization of the membrane. It is evident how a larger input current increases the spiking frequency. Furthermore, Fig. 3 illustrates how the parameter V_{thr} affects the spiking behavior, as a smaller V_{thr} reduces the current charging C_{mem}, resulting in a lower spiking frequency. Essentially, the voltage V_{thr} can determine what part of the input current I_{in} will be injected into the membrane [9].

In Fig. 4 the output spikes V_{spike}, together with the membrane voltage V_{mem} are demonstrated for the case of a spiking input current. Focusing on the V_{mem} waveform, the Leaky Integrate-and-Fire dynamics are clear, as the membrane

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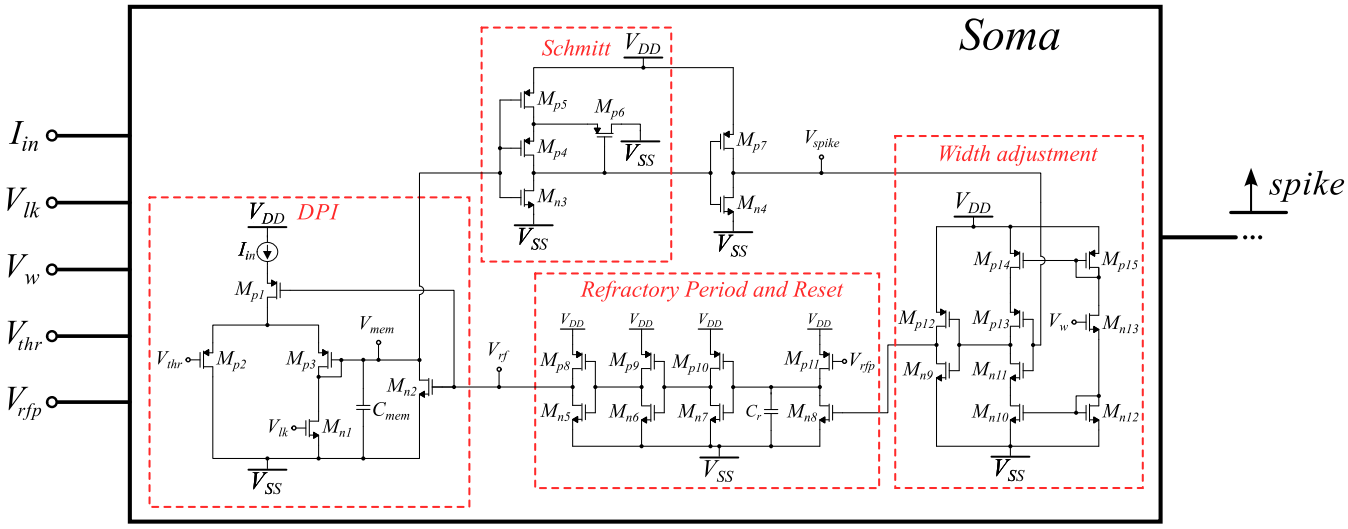

Fig. 1: Circuit diagram of the proposed modified neuron

capacitor C_{mem} charges with the arrival of the input pulse and then discharging through transistor M_{n1}.

In general, the proposed neuron exploits the simplistic dynamics of the DPI, combined with a suitable low-power comparator (1N3P Schmitt Trigger). The modified Schmitt Trigger ensures minimal power dissipation, especially as V_{mem} rises gradually, unlike a sharp edge, which can prove detrimental for power consumption. The width adjustment block and the refractory period block provide accurate control over the duration of the spike and the refractory period of the neuron, respectively [13]. The overall result is a versatile, highly-tunable neuron, which maintains low power consumption. Specifically, under a constant input current of $I_{in} = 10nA$ the spiking frequency is $44kHz$ (assuming the parameter values of Fig. 5) and the mean power of the neuron is $13nW$, making it ideal for integration in large neuromorphic networks.

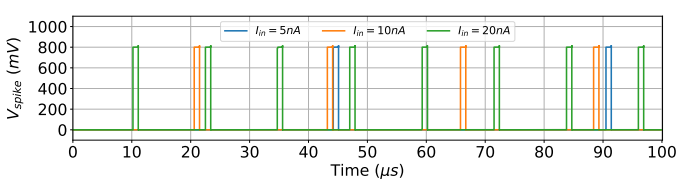

Fig. 2: Spiking output for constant input current (long depolarization). Bias parameters are $V_{thr} = 0.6V$, $V_{lk} = 0.2V$, $V_w = 0.45V$ and $V_{rfp} = 0.45V$.

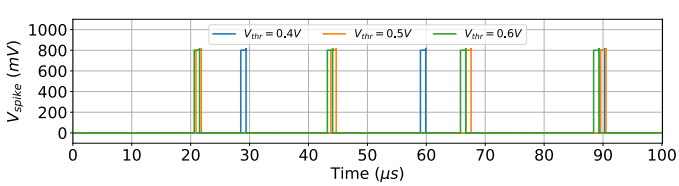

Fig. 3: Spiking output for different values of V_{thr}, demonstrating the various frequencies achieved. The rest of the parameters are $I_{in} = 10nA$, $V_{lk} = 0.2V$, $V_w = 0.45V$ and $V_{rfp} = 0.45V$.

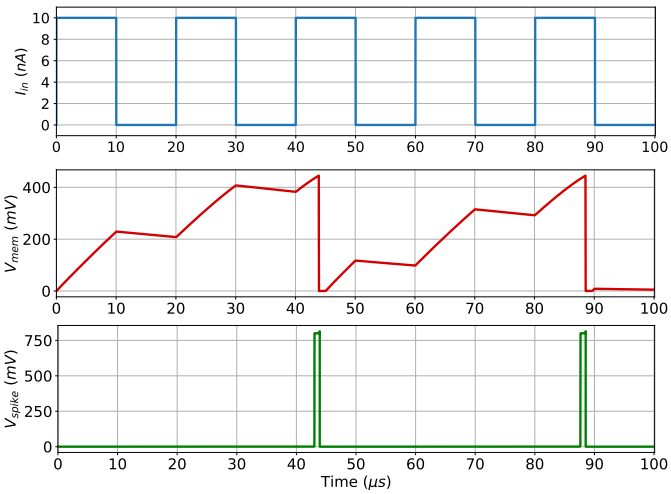

Fig. 4: Neuron's membrane voltage V_{mem} (middle), output spikes V_{spike} (bottom) for a spiking input current I_{in} (top). The bias parameters are $V_{thr} = 0.6V$, $V_{lk} = 0.2V$, $V_w = 0.45V$ and $V_{rfp} = 0.45V$.

IV. Comparison and Conclusion

Table I summarizes the performance of the proposed DPI based LIF neuron against state-of-the-art implementations. This comparison focuses on key neuromorphic parameters such as the energy efficiency, spike frequency, and tunability of critical parameters such as spike width and refractory period. The proposed 65 nm design achieves $20.42fJ/spike$ at $51.5kHz$ with independent tunability of the pulse width and the refractory period thus providing versatility in its usage in different encoding methods such as rate coding or time to first spike. This flexibility sets the proposed neuron apart from prior works that often trade off these features. Prior designs have achieved sub-$20fJ/spike$ but either lack independent refractory tuning or suffer from degrading accuracy in neuromorphic systems due to PVT variations. This degradation

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TABLE I: Comparison of different LIF neuron implementations.

	Technology node (nm)	Spike frequency (kHz)	Energy per spike (fJ)	Spike width tunability	Refractory tunability
This work	65	51.5	20.42	✓	✓
[10]	65	1.2	78.3	×	×
[12]	130	25	200	✓	✓
[13]	65	44	18.2	✓	✓
[16]	28	56	35	×	×
[17]	55	2	1099	✓	×

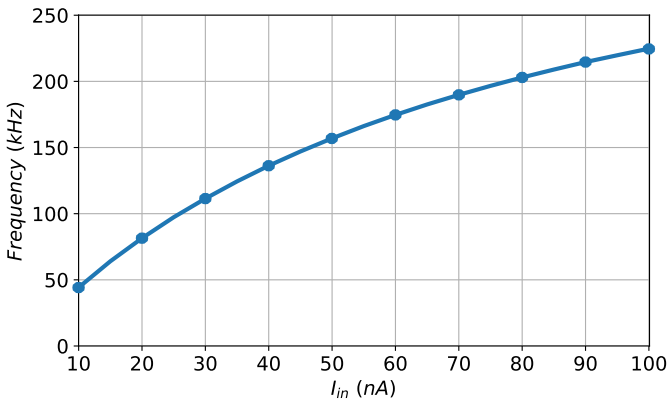

Fig. 5: Dependence of output spiking frequency f from the constant input current I_{in}. The bias parameters are $V_{thr} = 0.6V$, $V_{lk} = 0.2V$, $V_w = 0.45V$ and $V_{rfp} = 0.45V$.

arises because neurons with different pulse widths affected by process, voltage, and temperature mismatches produce inconsistent contributions to the next layer's integration. The proposed work achieves a balanced profile by delivering competitive energy efficiency alongside independent control of spike width and refractory period, ensuring robust timing stability for systems requiring flexible temporal dynamics.

In conclusion, the proposed DPI-based leaky integrate-and-fire neuron addresses two main challenges the ultra-low energy consumption and multi-parameter tunability, offering a flexible and robust solution for neuromorphic architectures. By leveraging subthreshold DPI dynamics for logarithmic membrane response and a leakage-reduced 1N3P Schmitt trigger, the proposed neuron achieves $20.42fJ/spike$ while enabling independent adjustment of spike width and refractory period features that provide flexibility in event-driven applications. Thus the proposed neuron is ideal for analog neuromorphic computing where tunable spike behaviors directly affect algorithmic needs.

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