# An Energy-Efficient Analog Integrated Neural Network for Cirrhosis Patient Survival Prediction

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***Abstract*—In this study, an energy-efficient analog integrated artificial neural network architecture is introduced. It comprises circuits operating in the sub-threshold region, including a ReLU circuit, a Sigmoid function circuit, an analog multiplier, and a current comparator. A Cirrhosis patient survival dataset is used to validate the proper operation of the proposed classifier. This classifier achieves an accuracy of $91.45\%$ while consuming only $924nW$. The design is implemented and validated using the TSMC $90$ nm CMOS process, with its post-layout performance benchmarked against both software implementations and existing works in literature. The architecture's robustness is verified through Monte Carlo simulations and corner analysis.**

***Index Terms*—analog integrated design, low-power architecture, ReLU-based design, artificial neural network**

## I. Introduction

Artificial Intelligence (AI) has experienced incredible growth over the past few years enabling machines to solve complex problems with incredible accuracy [1]. Those advancements, driven from the increase in data availability and great improvements in computing hardware and relevant algorithms, have facilitated innovative solutions in applications ranging from computer vision to natural language and biomedical data processing [2]. Machine Learning (ML) systems in particular can enable machines to carry out such tasks through an iterative learning process without being explicitly programmed to perform them. Artificial neural networks have nowadays emerged as one of the most successful and widely used machine learning model types due to their versatility and ability to incorporate efficiently very large amounts of data [2].

Historically the training and use of such ML models was carried out with digital circuits [3]. However, in recent years, analog AI hardware [4], which uses the continuous response of electronic circuits to perform complex mathematical operations, has emerged as an alternative computing technology for ML applications mainly due to its capability to offer substantially lower power consumption and better energy efficiency than comparable digital circuits. ML applications are especially suitable for analog computing [4] techniques due to their increased tolerance to noise and other random variations which enables them to take full advantage of the capabilities of such systems with minimal accuracy loss.

One of the most promising applications of analog ML Integrated Circuits (ICs) is that of implantable and wearable biomedical monitoring devices which need to operate reliably with very small power consumption [5], [6]. This constraint has made their implementation with traditional digital circuits very challenging, limiting them to mostly be able to use simpler and less accurate monitoring algorithms. Thus, analog computing [7] can allow such systems to implement very accurate ML models, increasing their effectiveness and allowing for better patient care. One prevalent condition whose long term treatment could greatly benefit from improved monitoring devices is Cirrhosis, which refers to scarring of the liver due to long-term damage that prevents it from functioning properly. In this work we introduce a classifier based on an integrated Analog Neural Network (ANN) for predicting the survival of Cirrhosis patients [8]. This hardware design is validated using a widely used Cirrhosis patient dataset and its performance is compared to relevant literature.

The following sections of this paper are structured as follows: Section II presents an overview of Artificial Neural Networks (ANNs). In Section III, the proposed architecture is analyzed, along with its fundamental structural elements and their operations. Necessary tests are conducted on the layout to validate the classifier's behavior, as outlined in Section IV. Section V provides a comparison with existing literature. The paper concludes with Section VI.

## II. Artificial Neural Network

Artificial Neural Networks (ANNs) are computational models inspired by the structure and function of biological neural systems. These models are made up of interconnected processing units called artificial neurons. Each neuron aggregates multiple inputs, applies a weighted sum, and then passes the result through a non-linear activation function to generate an output. These neurons are organized in multiple layers: typically an input layer, one or more hidden layers, and an output layer, forming a network capable of performing complex computations. Information flows through this network in a process known as feedforward propagation [9]. The learning process in ANNs is driven by backpropagation, a training algorithm that iteratively adjusts the connection weights to minimize prediction errors. This training enables ANNs to excel at various tasks, including classification, regression, pattern recognition, and signal processing, with applications in fields such as healthcare, finance, natural language processing, and image analysis [2].

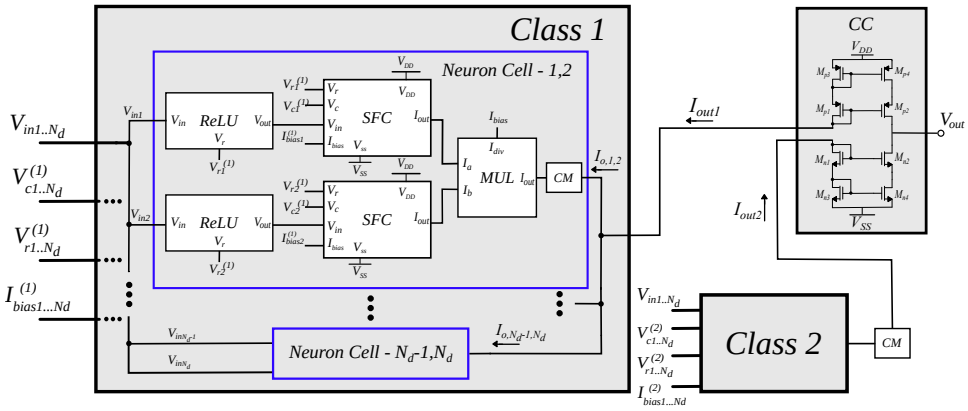


Fig. 1: The high-level architecture of the proposed system.

Mathematically, the function of ANNs can be described by three core components: weighted connections between neurons, aggregation of weighted inputs, and non-linear activation functions. The output $x$ of a neuron in a layer $l+1$ receiving input from $n$ neurons in the previous layer $l$ is given by:

$$x_i^{(l+1)} = f_\alpha(\sum_{k=1}^{n} w_{ki}^{(l)} x_k^{(l)} + b_i^{(l+1)}) \tag{1}$$

In this equation, $x_i^{(l+1)}$ represents the output of neuron $i$ in layer $l+1$. This neuron takes inputs from $n$ neurons in the previous layer, combines them into a weighted sum, and processes this sum. The weight connecting neuron $k$ (where $k \in [1, n]$) to neuron $i$ is denoted by $w_{ki}^{(l)}$, while $b_i^{(l+1)}$ represents a bias term for neuron $i$. The activation function, $f_\alpha$, then applies a transformation to the weighted sum, generating the neuron's final output.

## III. Proposed Architecture

This section introduces the design of the analog building blocks that compose the proposed neural network. A system designed to solve a classification problem that involves $N_d$ features split between two classes, as illustrated in Fig. 1, was selected to demonstrate the network's simplicity and efficiency across different input sizes while maintaining high accuracy. Each class is represented by a collection of neuron cells. In every neuron cell, two input features are independently processed by the architecture's main building blocks.

Initially, for each feature, the input voltage $V_{in,i}$, where $i \in [1, N_d]$, is applied to the ReLU circuit [10] shown in Fig. 2. This circuit is composed of two transistors $M_{p1}$ and $M_{p2}$ and compares the input and reference voltages $V_{in}$ and $V_r$ respectively. The output voltage takes the value of the higher potential. This configuration can effectively realize the ReLU function as shown by the waveform in Fig. 2.

The output of the ReLU function, alongside the training parameters $V_r$, $V_c$ and $I_{bias}$, are then connected to the input of the next analog building block, the Sigmoid Function Circuit (SFC) [11] shown in Fig.3. This design uses transistors $M_{n5}$ to $M_{n8}$ to realize a differential pair composed of composite transistors. This architecture splits the bias current $I_{bias}$ into sigmoid-shaped currents centered around the reference voltage ($V_r$). Furthermore, the control voltage $V_c$ connected to the bodies of transistors $M_{n5}$ and $M_{n6}$ adjusts the curve's width, enabling tunability. The selected sigmoid curve is the one transitioning from high to low and its magnitude is determined by the bias current.

The resulting currents of the two SFCs of the neuron cell are fed into the an analog multiplier [12], illustrated in Fig. 4, which multiplies the two values to produce the neuron's output. This implementation operates on the translinear principle in order to compute the product of input current $I_a$ and $I_b$. The produced product is normalized by the reference current $I_{div}$. The output current is given by $I_{out} = (I_a \cdot I_b)/I_{div}$. This design operates in the subthreshold region enabling the transformation of the gate to source voltages within the loop into the current product. This is possible due to the exponential behavior between the gate to source voltage and the drain current in the subthreshold region, making this design highly efficient while ensuring accurate current multiplication.

The resulting currents of each neuron cell are then summed to form the final output current of the corresponding class. To maintain proper signal routing between blocks, the design makes extensive use of Current Mirrors (CMs), ensuring that each block's output current flows correctly into the next stage. Finally, the Current Comparator (CC) block in Fig. 1 examines the class output currents and forces $V_{out}$ to swing to high or low based on which class dominates, thereby making the final decision.

## IV. Simulation Results and Data Analysis

The proper operation of the proposed architecture was verified using the Cirrhosis Patient Survival Prediction dataset, available on Kaggle [8]. The parameters in the dataset include a range of medical and demographic information, such as age, presence of ascites, hematomegaly, edema etc. Using this dataset researchers can develop predictive models for the survival chances of cirrhosis patients leading to the improvement of patient outcomes and medical diagnostics. It consists of 2 classes and $N_d = 17$ features. All experimental results were

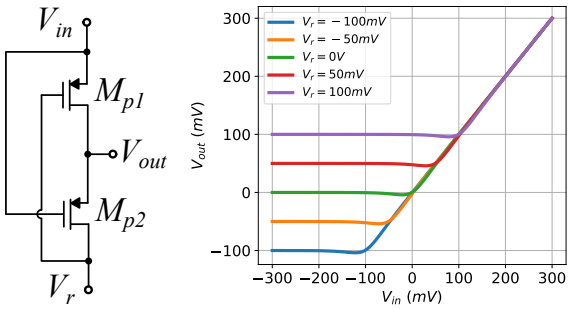


Fig. 2: The implementation of the Rectified Linear Unit (ReLU) circuit employs two PMOS transistors (shown on the left). The ReLU circuit's output is displayed on the right for a parametric sweep.

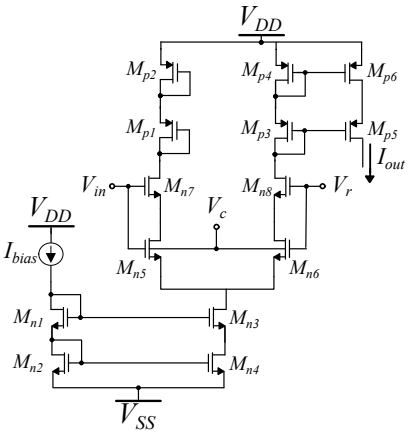


Fig. 3: The Implemented Sigmoid Function Circuit (SFC).

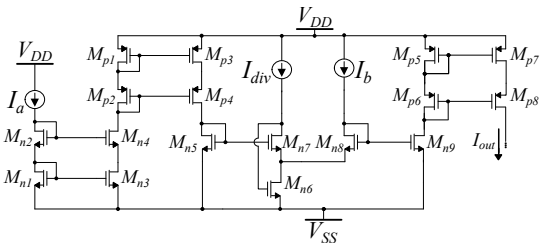


Fig. 4: The analog translinear implementation of the multiplier.

derived from the layout, shown in Fig. 5, realized through a TSMC 90nm CMOS process using Cadence Virtuoso.

To evaluate the proposed classifier's performance, two distinct tests were carried out. The first test assessed the impact of random effects during the training process, with 20 iterations performed for both software and hardware models, followed by a comparative analysis. The results are illustrated in Fig. 6. Additionally, to examine the behavior of the architecture under Process-Voltage-Temperature (PVT) variations a corner analysis was conducted. The corner analysis examines variations in Process (Typical, Slow, Fast), fluctuations in Temperature ($-25^oC$ to $125^oC$) and Voltage ranging from ($V_{DD} = -V_{SS} = 0.25$ V) to ($V_{medwith100iterations,andtheresultsarepresentedinFig.6.Theaboveoutcomes.measurethereliability androbustnessoftheproposedarchitectureacrossvariousc}$

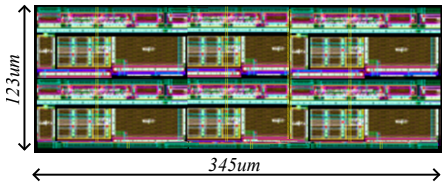


Fig. 5: The layout implementation of the proposed architecture consisting extra dummy transistors.

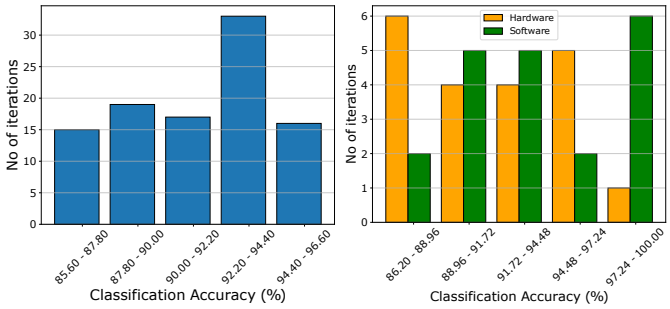


Fig. 6: Post-layout Monte-Carlo simulation results of the proposed architecture on the dataset (left). Classification outcomes of the proposed architecture and the equivalent software model on the dataset across 20 iterations (right).

## V. Comparison and Discussion

The primary objective of this study is to optimize the trade-off between energy efficiency, classification accuracy, and processing speed. As summarized in Table I, the proposed architecture demonstrates the lowest power consumption and energy per classification compared to existing solutions. All designs were implemented using the TSMC 90nm CMOS technology and evaluated on an identical dataset to ensure a consistent and fair performance comparison.

The proposed architecture offers robust accuracy with moderate complexity, striking a practical balance between performance and power usage. Although increasing the model's complexity could yield higher accuracy, it would come at the cost of significantly higher energy consumption. Given its efficiency and performance, the proposed architecture is well-suited for applications such as wake-up circuits in power-sensitive, high-accuracy digital machine learning systems.

## VI. Conclusion

In this study, a low-power analog integrated classifier for Cirrhosis patient survival prediction based on an ANN was introduced. The proposed architecture consists of analog circuits, which operate in the sub-threshold region to achieve low power consumption. Post-layout simulations conducted with the Cadence IC Suite using the TSMC 90nm CMOS technology confirm that the proposed analog classifier operates correctly with high accuracy (91.46%). The implemented classifier was trained using software and compared to related classifiers. Both Monte-Carlo and Corner analysis confirm the high robustness of the classifier over mismatches and PVT variations.

TABLE I: Comparison of analog classifiers on the classification dataset.

| | Classifier | Worst accuracy | Median accuracy | Max accuracy | Power consumption | Classification speed | Energy per classification | Complexity |
|---|---|---|---|---|---|---|---|---|
| **This work** | ANN | 86.20% | 91.45% | 97.80% | $924nW$ | $330K\,\frac{\text{classifications}}{\text{s}}$ | $\frac{2.8\text{ pJ}}{\text{classification}}$ | Medium |
| **[5]** | ANN | 84.80% | 89.33% | 95.50% | $2.78\mu W$ | $3M\,\frac{\text{classifications}}{\text{s}}$ | $\frac{0.927\text{ pJ}}{\text{classification}}$ | Medium |
| **[6]** | ANN | 87.40% | 91.55% | 95.90% | $4.21\mu W$ | $1.1M\,\frac{\text{classifications}}{\text{s}}$ | $\frac{3.83\text{ pJ}}{\text{classification}}$ | Medium |
| **[12]** | SVM | 87.30% | 89.22% | 92.70% | $69.77\mu W$ | $140K\,\frac{\text{classifications}}{\text{s}}$ | $\frac{498.36\text{ pJ}}{\text{classification}}$ | Medium |
| **[13]** | MLP | 96.00% | 98.55% | 99.80% | $451.78\mu W$ | $930K\,\frac{\text{classifications}}{\text{s}}$ | $\frac{485.78\text{ pJ}}{\text{classification}}$ | High |
| **[14]** | LSTM | 98.50% | 99.51% | 100.00% | $44.09mW$ | $870M\,\frac{\text{classifications}}{\text{s}}$ | $\frac{50.67\text{ pJ}}{\text{classification}}$ | High |
| **[15]** | RBF | 82.70% | 88.36% | 91.70% | $57.41\mu W$ | $200K\,\frac{\text{classifications}}{\text{s}}$ | $\frac{287.05\text{ pJ}}{\text{classification}}$ | Medium |
| **[16]** | K-means | 95.30% | 97.93% | 99.50% | $138.03\mu W$ | $5M\,\frac{\text{classifications}}{\text{s}}$ | $\frac{27.61\text{ pJ}}{\text{classification}}$ | High |
| **[17]** | Fuzzy | 82.30% | 89.03% | 93.70% | $1.053\mu W$ | $4.55K\,\frac{\text{classifications}}{\text{s}}$ | $\frac{231.43\text{ pJ}}{\text{classification}}$ | Medium |
| **[18]** | GMM | 81.70% | 88.57% | 93.20% | $1.851\mu W$ | $100K\,\frac{\text{classifications}}{\text{s}}$ | $\frac{18.51\text{ pJ}}{\text{classification}}$ | Medium |
| **[19]** | Threshold | 80.70% | 89.33% | 94.80% | $576nW$ | $100K\,\frac{\text{classifications}}{\text{s}}$ | $\frac{5.76\text{ pJ}}{\text{classification}}$ | Low |
| **[20]** | Bayes | 80.70% | 87.75% | 92.80% | $978nW$ | $100K\,\frac{\text{classifications}}{\text{s}}$ | $\frac{9.78\text{ pJ}}{\text{classification}}$ | Low |

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