# An Analog-Implemented Burst-Dependent Synaptic Plasticity Model for Hierarchical Neuromorphic Architectures

Vasileios Moustakas, Vassilis Alimisis, Anna Mylona, Francky Catthoor and Paul P. Sotiriadis
Department of Electrical and Computer Engineering,
National Technical University of Athens, 15780 Athens, Greece
and Archimedes, Athena Research Center, Greece.
E-mail: moystakasvasileios@gmail.com

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***Abstract*—Synaptic plasticity utilizing only pre- and post-synaptic spike timing is proven to be unreliable for credit assignments in deep, hierarchical networks. Recent theoretical work shows that synaptic plasticity through high-frequency postsynaptic bursts enables higher-order neurons to coordinate learning in lower layers through feedback pathways. In this work, we present a low-power analog implemented burst-dependent synaptic plasticity (BDSP) architecture that captures these principles in hardware. The proposed design integrates a low-power, two-compartment neuron capable of event and burst generation with synapses that detect and quantify bursts, compute long-term burst probability, and use it to adjust weights. This architecture is designed and tested using Cadence IC suite in a TSMC 65nm CMOS process. Results showcase that the proposed design can be the cornerstone of an energy-efficiency neuromorphic hierarchical architecture.**

***Index Terms*—Low power, Neuromorphic circuit design, Analog Neuron Cell, Burst dependent plasticity, Dendritic compartment**

## I. Introduction

The pursuit of biologically inspired computing has led to the development of neuromorphic systems that emulate neural mechanisms such as spiking activity and synaptic plasticity [1]. Among these, spike-timing-dependent plasticity (STDP) has played a central role in understanding and implementing learning processes in hardware and computational models [2]. STDP relies on the precise timing relationship between pre- and postsynaptic spikes to adjust synaptic weights, thereby enabling networks to learn temporal correlations [2]. However, while this mechanism performs effectively in shallow and feedforward networks, it fails to scale efficiently to deeper architectures, where reliable credit assignment across multiple layers becomes essential for complex learning tasks [3].

Recent theoretical advances in neuroscience have highlighted the importance of burst-based signaling as a complementary mechanism to classical STDP [2], [4]. Unlike single spike events, bursts, short sequences of high-frequency spikes, can convey richer information about neuronal activity and relevance [5]. Bursts have been shown to play a critical role in attention modulation, feedback signaling, and hierarchical learning in biological systems [6]. This burst-dependent communication allows higher-order neurons to influence synaptic changes in preceding layers, effectively addressing the problem of credit assignment in multilayer networks [6], [7].

In addition to their biological relevance, burst-based mechanisms offer significant advantages for hardware implementations [4]. Bursts inherently encode temporal information in a compact, energy-efficient manner, allowing analog and mixed-signal circuits to exploit event-driven computation with reduced power overhead [8]. Moreover, by differentiating between single spikes and bursts, neuromorphic systems can prioritize relevant events and suppress noise, improving learning robustness [9]. These properties make burst-dependent plasticity particularly well-suited for low-power neuromorphic architectures, where energy efficiency, adaptability, and compact circuit design are of primary importance [10].

Motivated by these insights, this work introduces a low-power, analog burst-dependent synaptic plasticity (BDSP) architecture that captures the essence of burst-mediated learning in hardware. The proposed design incorporates a two-compartment neuron capable of both event-driven and burst-mode operation, along with synaptic circuits that detect and quantify burst activity. These synapses compute the long-term burst probability and use it to modulate synaptic weights adaptively. Implemented and evaluated using the Cadence IC design suite in a TSMC 65 nm CMOS process, the architecture demonstrates efficient burst detection and learning behavior while maintaining low power consumption. The presented results present that this BDSP framework can serve as a foundational element for scalable, energy-efficient neuromorphic systems capable of hierarchical learning.

To the best of the authors' knowledge, this is the first implementation of BDSP in analog integrated circuits. The proposed synaptic circuit is entirely novel and specifically tailored to the BDSP learning rule, its operation is inherently algorithm-dependent rather than derived from any pre-existing synaptic models. This algorithm-specific synapse enables the realization of burst-based learning directly in hardware, marking a significant departure from prior analog and digital implementations. Furthermore, the proposed neuron is fully tunable, allowing independent control of its refractory period and spike width, which provides flexibility in emulating diverse neuronal

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behaviors. Together, these features establish a new class of tunable, algorithm-driven analog neuromorphic circuits that advance the state of the art in low-power learning architectures.

The remainder of this paper is structured as follows: Section II introduces the background theory of burst-dependent synaptic plasticity. Section III details the proposed low-power analog implemented burst-dependent synaptic plasticity and its constituent subcircuits. Section IV presents the simulation results and performance evaluation. The paper concludes with closing remarks in Section V.

## II. Burst-Dependent synaptic plasticity

BDSP represents a biologically grounded learning mechanism that utilizes burst firing to address the credit assignment challenge in layered spiking neural systems [6], [11]. The framework relies on a dual-compartment neuron structure, a fundamental element that governs its behavior. The basal compartment processes incoming feedforward signals and generates somatic action potentials, while the apical compartment integrates feedback signals from higher cortical areas. When the apical compartment becomes sufficiently excited, it evokes a somatic high-frequency burst, typically characterized by two or more spikes with an interspike interval shorter than a specific limit (for instance, $400\mu S$). The initial spike within this burst is treated as an event, creating a temporally structured sequence of synaptic plasticity operations: the first event initiates long-term depression (LTD), followed immediately by the burst itself, which produces long-term potentiation (LTP). In Fig. 1, it is shown that regardless of the activity

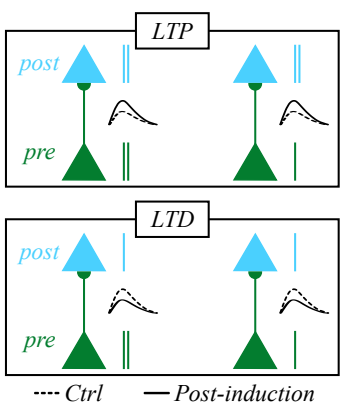


Fig. 1: Learning rule diagram illustration LTP and LTP depending on bursts or events

of the previous neuron, what matters is whether the postsynaptic neuron produces a burst or an event, which determines whether LTP or LTD occurs. By design, the amplitude of LTP outweighs the initial LTD, ensuring that a burst leads to an overall enhancement in synaptic strength. This architecture allows descending (top-down) signals to influence neuronal output modes directly and to replace ongoing depression with a stronger instructive potentiation signal.

The synaptic weight update rule is event-driven and local, requiring only signals available at the synaptic site [6]. The change in a synaptic weight $w_{ij}$ is given by

$$\frac{dw_{ij}}{dt} = \eta[B_i(t) - \Theta E_i(t)]\tilde{E}_j(t), \tag{1}$$

where $B_i(t)$ and $E_i(t)$ correspond to the postsynaptic burst and event trains, respectively. The variable $\tilde{E}_j(t)$ denotes a presynaptic eligibility trace that encapsulates a decaying record of prior presynaptic activity, identifying the synapse as eligible for modification. The constant $\Theta$ is a threshold parameter that balances potentiation and depression dynamics. Under this rule, a postsynaptic burst $B_i(t)$ induces LTP at synapses exhibiting a non-zero eligibility trace, while a postsynaptic event $E_i(t)$ induces LTD. The interplay between these processes ensures that bursts drive a net synaptic strengthening effect.

This biologically plausible learning rule enables a powerful computational approach to hierarchical learning: feedback signals, conveyed through apical activation, regulate burst production and consequently the sign and magnitude of synaptic plasticity in feedforward circuits [6]. The BDSP model thus provides a compact, hardware-efficient realization of top-down guided synaptic adaptation, approximating gradient-based learning while avoiding the biologically unrealistic assumptions of global error backpropagation.

## III. Proposed Circuit Architecture

This section presents the overall architecture, building blocks, and learning rule of the proposed Burst-Dependent Synaptic Plasticity (BDSP) model. The BDSP mechanism is implemented using a fully analog, two-compartment neuron and synapse design that is based on biological interaction between somatic and dendritic compartments. The main design concerns are tunability, robustness, and low-power consumption to ensure reliable operation across a wide input range.

The neuron and synapse circuits are designed to be tunable, supporting multiple adjustment schemes. The neuron's primary parameters, such as refractory period, leakage rate, and spike width, are fully adjustable, making the circuit flexible enough to support various Poisson spike trains. This tunability enables accurate control of interspike intervals (ISI) and the generation of bursts, ensuring correct emulation of a modified BDSP learning algorithm without degradation of performance or energy efficiency. By leveraging the advantages of analog circuits, the proposed architecture learns in an event-driven manner without the overhead of local control logic. The local interaction between neuron dynamics and a trace eligibility mechanism permits burst detection and weight modification, thereby exercising burst-dependent plasticity.

### A. Lif Neuron Circuit

The transistor-level circuit of the proposed leaky integrate-and-fire neuron is shown in Fig. 2. Previous implementations have employed Schmitt trigger–based hysteresis comparators [12], [13] to realize leaky integrate-and-fire (LIF) neuron circuits. However, these designs typically lack refractory-period tunability and offer only limited control over output pulse width [14] while others struggle with high power consumption

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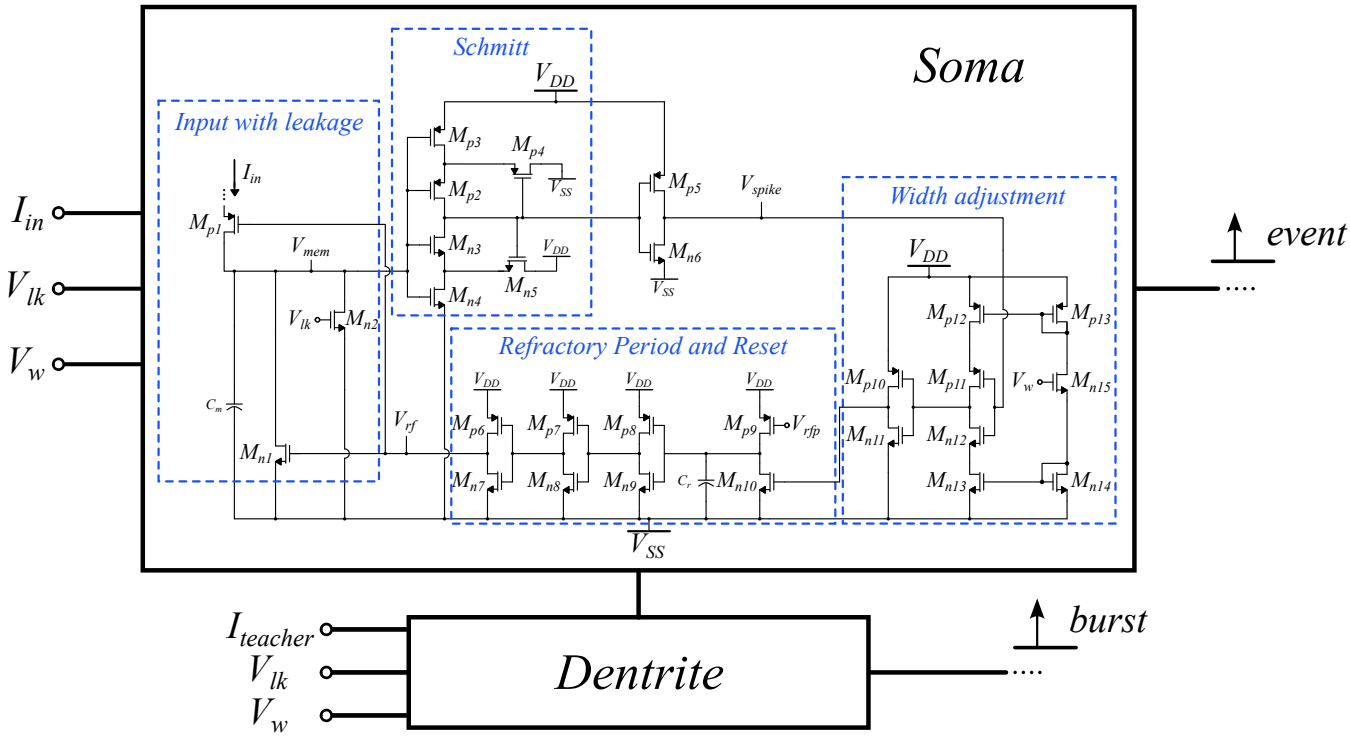


Fig. 2: Circuit diagram of the proposed two-compartment LIF neuron

[15], [16]. It consists of four main sub-circuits. The input leaky integrator circuit, a hysteresis comparator implemented as a Schmitt trigger, a current-starved inverter to control the output spike's width, and a reset and refractory control circuit.

The leaky integrate circuit accumulates the input current from previous neurons or the input Poisson spike train, while leaking over time through the leakage transistor $M_{n2}$. Similar to a biological neuron, the leakage current $I_{lk}$ continuously draws the membrane potential $V_{mem}$ back toward its resting potential. Thus, in the absence of spiking activity, the electrical charge accumulated on the membrane capacitor gradually dissipates over time towards the resting voltage $V_{SS}$.

The hysteresis comparator (Schmitt trigger) is implemented by transistors ($M_{n3}$ to $M_{n5}$) and ($M_{p2}$ to $M_{p4}$). It tests the membrane potential $V_{mem}$ against two distinct thresholds, one for the rising and one for the falling input. When the membrane voltage crosses the upper threshold, the hysteresis comparator produces a digital-like low signal equal to $V_{SS}$, and when it drops below the lower threshold, the output switches back to a high signal equal to $V_{DD}$. This hysteresis behavior prevents rapid switching due to small input fluctuations, ensuring stable and noise-resilient signal transitions.

The output of the Schmitt trigger is passed through an inverter to change the polarity and produce the output spike. This signal is the input to a current-starved inverter to introduce a controllable delay to a pulse signal, enabling precise adjustment of its pulse width. The circuit operates by restricting the current supplied to the CMOS inverter through the control bias voltage $V_w$ and transistors ($M_{n11}$ to $M_{n15}$) and ($M_{p10}$ to $M_{p13}$) that act as current sources. By starving the inverter of current, the rise and fall times of the output signal are intentionally slowed, and the propagation delay of the inverter is prolonged. This delay directly determines the pulse duration, so its width can be controlled on a fine scale simply by adjusting the control voltage driving the bias transistors. This circuit thus shows an efficient and compact method of providing pulse shaping.

The inverted output of the current-starved inverter is routed to the Refractory and Reset subcircuit, which is composed of the transistor pairs ($M_{n7}$ to $M_{n10}$) and ($M_{p6}$ to $M_{p9}$) and the refractory capacitor $C_r$.When a trigger signal from the pulse width adjustment block arrives, $C_r$ is rapidly discharged and then gradually recharged through transistor $M_{p9}$ , whose gate is biased by the control voltage $V_{rfp}$. This voltage defines the charging current and thereby sets the time constant of the refractory period. As $C_r$ charges, its voltage is continuously compared to the switching threshold of the inverter pair ($M_{n9}$ and $M_{p8}$), and the resulting waveform is buffered through transistors ($M_{n7,8}$ and $M_{p6,7}$) to produce a clean refractory control signal. During this interval ($V_{cr} < V_{th}$) the refractory node $V_{fr}$ is held at $V_{DD}$. This forces the membrane voltage to $V_{SS}$ through $M_{n1}$ and forces $M_{p1}$ into the cutoff region, isolating the soma from incoming input currents. Consequently, the neuron remains inactive and does not respond to external spikes while the refractory period is active.

The dendritic compartment employs the same circuit topology as the somatic unit, with the only distinction being its input source, which originates from a top-down or teacher signal representing contextual or supervisory feedback. In the proposed system, a burst event is defined as a coincident

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activation of both the dendritic and somatic compartments. This dual-trigger condition ensures that a burst is generated only when feedforward excitation (from the soma) and feedback modulation (from the dendrite) occur simultaneously. By enforcing this coincidence requirement, the circuit effectively prevents false potentiation that could otherwise arise from high-frequency Poisson inputs producing multiple somatic spikes within the ISI window. Consequently, only spikes that are both temporally correlated and contextually validated by the dendritic input are classified as bursts and contribute to synaptic strengthening.

### B. Synapse

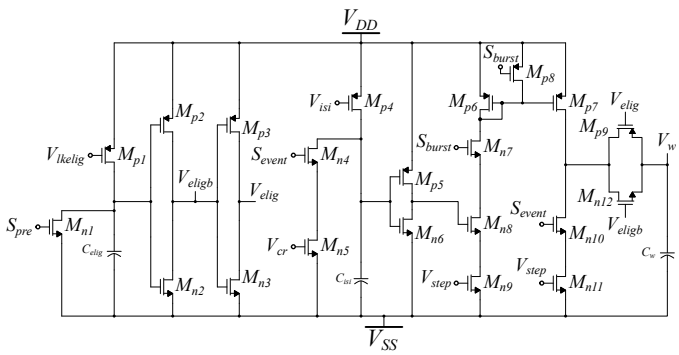


Fig. 3: Circuit diagram of the proposed synapse

The proposed synapse, illustrated in Fig. 3, implements the burst-dependent synaptic plasticity rule discussed in Section II. The eligibility trace is represented by the capacitor $C_{elig}$, which is discharged when a pulse from the presynaptic input arrives and subsequently recharged through transistor $M_{p1}$. This charging and discharging behavior defines the temporal dynamics of the eligibility trace, which in turn controls the gates of the transmission pair $M_{p9}, M_{n12}$. The transmission gate remains conductive only during the active eligibility period, thereby ensuring that synaptic modulation occurs exclusively within this biologically relevant time window.

The implemented learning algorithm follows the burst-dependent plasticity principle in which each postsynaptic activation is first classified as an event, corresponding to a single spike that may or may not evolve into a burst. When a postsynaptic spike occurs, an interspike-interval (ISI) detection window is initiated, during which the circuit performs a preliminary LTD operation. If no subsequent spike is detected within this window, the activation remains classified as an event, and the synaptic weight $V_W$ decreases. However, if an additional spike occurs within the ISI window, the activation is reclassified as a burst, and the synapse transitions to LTP.

In the proposed hardware implementation, this behavior is realized through charge-based modulation of the weight capacitor $C_w$. During an event, $V_w$ decreases as $C_w$ is discharged though transistors $M_{n10,11}$. Simultaneously, the ISI window opens and is defined by the capacitor $C_{ISI}$, which is discharged by transistors $M_{n4,5}$ and recharged by $M_{p4}$,and compared to the switching voltage of the inverter ($M_{p5}$, $M_{n6}$) setting a time window of $400\mu$s. Transistor $M_{p8}$ serves to hold the gates of the current-mirror pair ($M_{p6}, M_{p7}$) at $V_{DD}$ during the interspike interval, thereby preventing unwanted leakage currents and ensuring that the mirror remains inactive while the neuron is in its depression phase. When a second spike is detected within the ISI window, $M_p8$ turns off and $M_{n7}$ conducts, enabling the charging path for the weight capacitor $C_w$ through transistor $M_{p7}$. This action initiates the potentiation phase associated with burst detection. It is important to note that the current mirror ($M_{p6}, M_{p7}$) is designed with a 1:2 ratio, providing a higher charging current during LTP than the discharging current applied during LTD. This asymmetric configuration ensures that the potentiation induced by the burst sufficiently compensates and surpasses the prior depression caused by the initial event, resulting in a net increase in synaptic weight.

## IV. Simulation Results

The proposed BDSP architecture is designed and verified using the TSMC 65 nm CMOS process. The transistor dimensions in Fig. 2 are $(W/L) = 200\text{nm}/200\text{nm}$ for NMOS transistors and $(W/L) = 300\text{nm}/200\text{nm}$ for PMOS transistors, except for $M_{p10}$, $M_{p11}$, $M_{n11}$, and $M_{n12}$, which have $(W/L) = 500\text{nm}/200\text{nm}$. In addition, $M_{n10}$ has $(W/L) = 200\text{nm}/500\text{nm}$. The transistor dimensions in Fig. 3 are $(W/L) = 200\text{nm}/200\text{nm}$ for NMOS transistors and $(W/L) = 300\text{nm}/200\text{nm}$ for PMOS transistors, except for $M_{p7}$, which has $(W/L) = 600\text{nm}/200\text{nm}$. Also, the power supply rails for the BDSP are equal to $V_{DD} = 0.8V$ and $V_{SS} = 0V$.

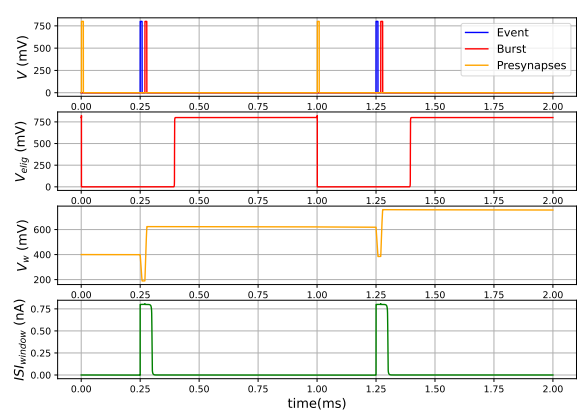


Fig. 4: Timing diagram of LTP and LTD

Fig. 4 illustrates the timing behavior of the proposed synapse circuit. The first row shows the arrival times of the pre-synaptic pulse along with the corresponding event and burst signals generated at the postsynaptic neuron. The second row depicts the voltage $V_{elig}$, which serves as the control input for the PMOS transistors; the eligibility period is active when $V_{elig}$ is held at $V_{SS}$. The third row presents the resulting LTD and LTP signals, indicating synaptic depression and

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potentiation events that occur following the arrival of an event or a burst, respectively. Finally, the fourth row illustrates the interspike-interval (ISI) window, which defines the temporal threshold used to classify postsynaptic activations as either isolated events or bursts.

In Figs. 5 and 6, the neuron is simulated under long depolarization conditions and high frequency spike train. In Fig. 5, a high frequency input pulse (green) is applied, and the output (yellow) shows that the membrane potential charges up to a certain level and then exhibits a sequence of spike–refractory–spike–refractory cycles. In Fig. 6, a similar behavior is observed, but with a lower frequency input pulse. The proposed neuron demonstrates proper leak behavior under both high-frequency long-depolarization spike trains and spike trains where the membrane voltage ($V_{\mathrm{mem}}$) increases and then decreases during the refractory period. In the top figure, the membrane potential reaches the threshold of the Schmitt trigger, generating a spike (blue curve), after which the neuron fires (integrate-and-fire behavior) and enters a refractory period (red region). The same mechanism is observed in the bottom figure, where multiple pulses result in both integrate-and-fire and leak responses.

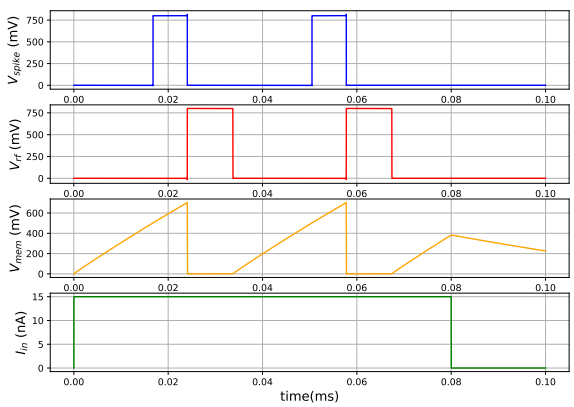


Fig. 5: Operation of the neuron under long depolarization

Fig. 7 demonstrates that the output pulse width of the neuron can be modulated by varying the control bias voltage $V_w$ of the current-starved comparator. This tunability is advantageous, as biological neurons commonly encode information through the timing and duration of action potentials. By adjusting the pulse width, the circuit can replicate various temporal coding schemes, such as rate coding, time to first spike, and burst coding [17], [18]. Consequently, this feature enables the investigation of temporal dynamics for achieving more biologically realistic and computationally efficient neuromorphic systems.

Fig. 8 demonstrates that the refractory period of the neuron can be modulated by varying the control bias voltage $V_{rpf}$. The fact that this circuit demonstrates this tunability over the refractory period is critical as it governs the neuron's firing rate, spike timing, and overall temporal dynamics. In

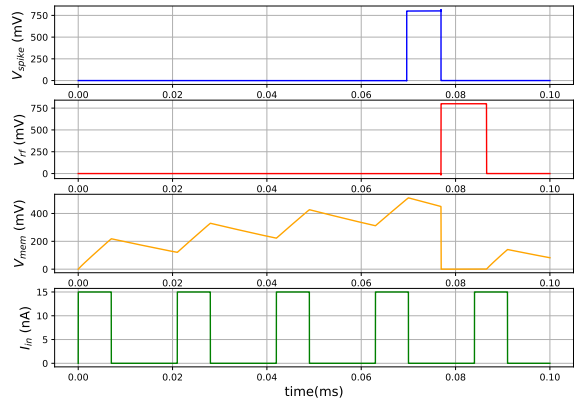


Fig. 6: Operation of the neuron under high frequency spike trains

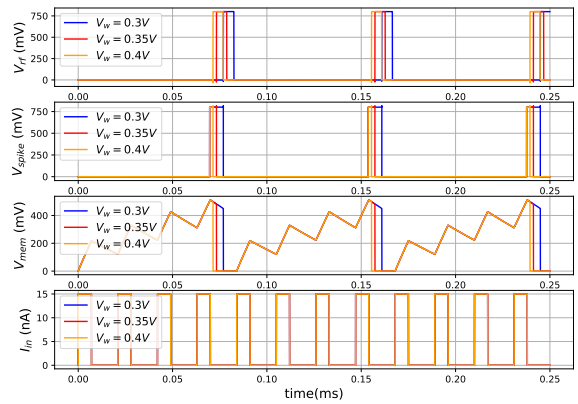


Fig. 7: Neuron's Width adjustment by modulating the bias voltage $V_w$ while keeping all the other biases constant

biological systems, the refractory period regulates the minimum interval between spikes, ensuring stability and preventing excessive firing [19], [20]. In analog neuromorphic systems, it contributes to energy-efficient operation by suppressing redundant spiking activity. Therefore, adjustable refractory mechanisms are critical for achieving both biologically realistic and computationally efficient neuromorphic systems.

## V. Conclusion

In this work, a BDSP architecture was presented, demonstrating hardware-based learning driven by burst activity rather than simple spike timing. The analog implementation of a two-compartment neuron, capable of both event and burst generation, efficiently interfaced with synapses designed to detect bursts, compute long-term burst probability, and adjust synaptic weights accordingly. Designed and verified using the Cadence IC design suite in a TSMC 65 nm CMOS process, the architecture achieved low power consumption while maintaining accurate burst detection and adaptive weight modulation. The results confirmed that the BDSP approach provided a

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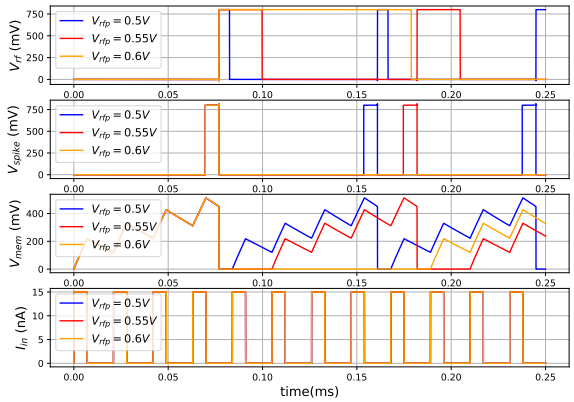


Fig. 8: Neuron's refractory period adjustment by modulating the bias voltage $V_{rfp}$ while keeping all the other biases constant

practical and energy-efficient hardware realization of burst-mediated learning. Overall, the demonstrated performance showed that this architecture could serve as a robust foundation for scalable, low-power neuromorphic systems capable of hierarchical learning and processing.

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