MINAR: Mechanistic Interpretability for Neural Algorithmic Reasoning

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Abstract

Graph neural networks (GNNs) are known to be capable of implementing specific algorithmic steps that guarantee strong out-of-distribution performance, a property referred to as *algorithmic alignment* or *neural algorithmic reasoning* (NAR). At the same time, recent advances in the reasoning capabilities of large language models (LLMs) have created an interest in *mechanistic interpretability*: identifying specific model components that are responsible for certain tasks. In this work, we adapt circuit discovery methods from mechanistic interpretability to the GNN setting with **M**echanistic **I**nterpretability for **N**eural **A**lgorithmic **R**easoning (MINAR). We validate MINAR by applying it to two GNNs: one predicting single-source shortest path distances and another computing shortest path distances and reachability in parallel. Through both examples, we demonstrate how mechanistic interpretability can offer fine-grained insight into an algorithmically aligned model. Our code will be made available at `https://github.com/he-jesse/minar`.

1 Introduction

The recent surge in the capabilities of large language models (LLMs) has created a commensurate demand for novel interpretability methods suited to analyze these models. At the same time, the discovery of phenomena like *grokking* [13] has shown that surprising structure arises in trained models. This confluence of interests has led to the emergence of *mechanistic interpretability* [9]: attempting to reverse-engineer a model's behavior in terms of its internal processes. At the same time, researchers have noticed that graph neural networks (GNNs) are capable of implementing specific algorithms. This is thought to be a result of the resemblance between their message-passing structure and dynamic programming. This notion, dubbed "algorithmic alignment" [17] or "neural algorithmic reasoning" [16], promises robust out-of-distribution generalization and substantial improvements in sample complexity. With an interest in discovering how models perform specific algorithmic tasks on the one hand, and a class of models that implement specific algorithms on the other, the algorithmic alignment of graph neural networks creates a natural testbed for fine-grained mechanistic interpretability research.

In this work, we introduce **M**echanistic **I**nterpretability for **N**eural **A**lgorithmic **R**easoning (MINAR), a method to identify neuron-level circuits in GNNs using circuit discovery methods like EAP [15] and EAP-IG [5]. To our knowledge, MINAR is the first attempt to bring mechanistic interpretability to the GNN setting. We apply our method to two GNNs: one predicting single-source shortest path distances and another computing shortest path distances and reachability in parallel. In the first, we validate our method by identifying the circuit that implements the Bellman-Ford algorithm. In the second, we identify that the model learns Bellman-Ford, but recycles much of the shortest path computation to predict reachability. These examples demonstrate how neuron-level circuits can offer detailed insight to trained models.

2 Related Work

Circuit Discovery and Mechanistic Interpretability Early mechanistic interpretability work (e.g., [9, 21]) combines manual examination of parameters with expert hypotheses to reverse-engineer the inner workings of a narrow trained model. However, the rise in language model capabilities has created an interest in applying such methods to much larger models. To this end, recent work has focused on methods to partially or totally automate much of the mechanistic interpretability process, detecting specific model components that are responsible for certain tasks. Such components and their connections are dubbed a "circuit" by Olah et al. [11], and the process of identifying circuits is known as *circuit discovery*. A number of approaches for circuit discovery have been proposed, broadly performing some form of activation patching [15, 5, 20] or pruning [1, 2, 19]. These methods formulate the model as a *computation graph* and attempt to find small subgraphs that are responsible for a particular behavior. To date, much of the circuit discovery literature has been focused on sub-tasks for language models such as indirect object identification or detecting which of two numbers is greater, and identifies coarse-grained circuits whose nodes are entire attention heads or MLP modules.

Algorithmic Alignment in Graph Neural Networks While mechanistic interpretability has revealed surprising structure in large generalist models, a particular class of narrow models has also been shown to possess algorithmic "reasoning" capabilities: graph neural networks. Broadly, GNNs operate on graph data via an iterative *message-passing* scheme: each node in the graph has an embedding, and at each layer of the network, each node will aggregate the embeddings of its neighbors and use the aggregated embeddings to update its own embedding. Xu et al. [17] and Dudzik and Veličković [3] point out that this aggregate-and-update flow resembles dynamic programming, hypothesizing that the *algorithmic alignment* of graph neural networks affords them an advantage in learning algorithmic tasks like single-source shortest path computation. Further, Veličković et al. [16] show that learning BFS and Bellman-Ford in parallel can help GNNs generalize on both tasks. However, it was only recently that Nerem et al. [10] showed that GNNs are not only *capable* of learning specific algorithms, but that a properly designed GNN will *provably* learn a specific algorithm (in this case Bellman-Ford) during training.

3 Preliminaries

It will be necessary to disambiguate the term "computation graph," which researchers define differently in the circuit discovery and in the graph neural network literature. Let Φ be a GNN operating on a graph $G = (V, E, X, A)$, where V is the node set, E is the edge set, $X : V \to \mathbb{R}^p$ are the node features and $A : E \to \mathbb{R}^q$ are edge attributes. Where necessary, we will denote by Ψ an arbitrary (perhaps non-graph) neural network.

In the circuit discovery literature [2, 15, 20], a "computation graph" (which we will call a *model computation graph*) refers to a graph representing individual model components. These model components are typically defined at an architectural level, rather than at the mathematical level. While earlier circuit discovery work defines these components at a lower resolution (e.g., entire attention heads or feedforward MLP modules), we consider circuits at the level of individual neurons.

Definition 3.1 (Model Computation Graph)**.** Let Ψ be a neural network with arbitrary subcomponents ψ_i. The *model computation graph* of Ψ, denoted $G_C^m(\Psi)$, is the directed graph with vertices i and edges (i, j) if the output of ψ_i is part of the input to ψ_j.

In graph neural network literature, some authors [18, 6] use "computation graph" to represent the layered message-passing performed by a GNN. We first briefly recall the message-passing scheme that underlies most popular GNNs. A GNN Φ of depth L maintains an embedding $\Phi_v^{(\ell)}$ for each node $v \in V(G)$ and $\ell = 0, \dots, L$, with layer 0 being the input node features $\Phi_v^{(0)} = X_v$. Each subsequent layer is given by

$$\Phi_v^{(\ell+1)} = f_{\mathrm{Up}}^{(\ell)}\left(\Phi_v^{(\ell)}, \bigoplus_{(u,v)\in E(G)} f_{\mathrm{Agg}}^{(\ell)}(\Phi_u^{(\ell)})\right) \tag{1}$$

where $f_{\mathrm{Agg}}^{(\ell)}$ and $f_{\mathrm{Up}}^{(\ell)}$ are any function and $\bigoplus$ denotes any permutation-invariant operation such as sum, mean, minimum, or maximum. We may denote the output of Φ at node v by Φ_v or $\Phi_v(G)$, if the input graph is ambiguous.

Definition 3.2 (Message-Passing Computation Graph)**.** Let Φ be an L-layer GNN operating on a graph G. Then the *(message-passing) computation graph* $G_c^v(\Phi)$ for Φ at $v \in G$ is the directed graph with nodes $\bigsqcup_{\ell=0}^{L} \mathcal{N}^{(\ell)}(v)$ and edges $(i^{(\ell-1)}, j^{(\ell)})$ for each $(i,j) \in E(G)$ if $j \in \mathcal{N}^{(L-\ell)}(v)$ where $\mathcal{N}^{(\ell)}(v)$ denotes the ℓ-hop neighborhood of v.

In what follows, we will follow the circuit discovery literature and use "computation graph" to refer to the model computation graph. Furthermore, we will consider circuit discovery at the neuron level: each node in the computation graph corresponds to an individual neuron in the model, and each edge corresponds to a connection between neuron activations.

4 Circuit Discovery for GNNs

Having introduced our definitions and notation, we introduce the scoring methods EAP [15] and EAP-IG [5], both forms of *attribution patching*. The goal of attribution patching is to approximate the difference in prediction that would occur if an edge in the computation graph was corrupted or removed [5]. Actually removing the edge and obtaining the result with a full forward pass is referred to as *activation patching* [2]. Our choice to use attribution patching rather than activation patching is in large part due to efficiency, as our neuron-level computation graphs are typically very dense. We also describe in this section our approach to discovering neuron-level circuits in the GNN setting.

4.1 Attribution Patching Scores

We will use the model computation graph using a single node prediction as the output, with the aggregated neighbor information appearing as additional inputs. We adopt the method of edge attribution patching (EAP) [15] and its integrated gradients variation EAP-IG [5]. Formally, let (i,j) be an edge in the computation graph of a neural network Ψ, corresponding to the connection between two modules ψ_i and ψ_j. The attribution score of (i,j) for a prediction $\Psi(x)$ takes the activation z_i at ψ_i for the input x together with the activation z_i' from a corrupted input x'. Then, given a loss L which measures the distance between predictions $y = \Psi(x)$ and $y' = \Psi(x')$, the EAP score uses the gradient of L with respect to the output of ψ_j. That is,

$$\mathrm{EAP}_{(i,j)}(x,x') = (z_i' - z_i)^\intercal \frac{\partial}{\partial \psi_j} L(\Psi(x), \Psi(x')). \tag{2}$$

Equation (2) comes from the first-order term in a Taylor expansion for the perturbation performed by activation patching. By perturbing the input and using the intermediate activations, EAP scores can be computed more efficiently than activation patching scores: EAP performs just two forward passes and one backwards pass for each pair of inputs [15].

EAP-IG [5] adapts EAP to use the integrated gradients method of [14], approximating an integral over the straight-line path between z_i and z_i' with a Riemann sum of m terms:

$$\text{EAP-IG}_{(i,j)}(x,x') = (z_i' - z_i)^\intercal \frac{1}{m} \sum_{k=1}^{m} \frac{\partial}{\partial \psi_j} L\left(\Psi(x), \Psi\left(x' + \frac{k}{m}(x - x')\right)\right). \tag{3}$$

EAP-IG is m times slower than EAP, essentially performing the EAP calculation m times for each pair of inputs [5].

4.2 Circuit Identification in GNNs

Because a graph neural network operates on each node of the input graph, EAP and EAP-IG assign each computation edge a different score for each input node in the graph. To give each computation edge a single score for a given prediction, MINAR sums over the scores from each vertex to obtain the total score for each computational edge on one graph instance. That is,

$$\mathrm{EAP}_{(i,j)}(G, G') = \sum_{v \in G} \left({z'}_i^{v'} - z_i^v \right)^\intercal \frac{\partial}{\partial \psi_j} L(\Phi_v(G), \Phi_{v'}(G')) \tag{4}$$

where z_i^v is the activation of neuron ψ_i on node v. We compute EAP-IG in a simlar manner, again summing over nodes to give a total score on a single graph instance. For EAP-IG, we implement the steps between the original and corrupted inputs by interpolating between all node and edge features.

Finally, since attribution scores are typically averaged over multiple input instances to understand their behavior across a probing dataset, we average over each input graph to obtain the final attribution score for each edge. We also follow previous work in using the absolute value of each attribution score for downstream circuit discovery:

$$\mathrm{EAP}_{(i,j)} = \left| \frac{1}{|\mathcal{G}_{\text{probe}}|} \sum_{(G,G') \in \mathcal{G}_{\text{probe}}} \mathrm{EAP}_{(i,j)}(G, G') \right| \tag{5}$$

and similarly for EAP-IG. We note that the summation in (4) can be replaced by any pooling operation (e.g. mean). We choose summation to mirror the test loss (9) in Section 5.1 is computed, following Nerem et al. [10].

To guarantee connectedness of the identified circuit, we propose to construct the circuit from complete paths between the computation graph's inputs and outputs. While previous work in circuit discovery uses naive top-k selection [15] or a greedy Dijkstra-like algorithm [5], these methods often produce parentless or childless edges which must then be pruned. Instead, MINAR takes advantage of the fact that the computation graph is directed, acyclic, and topologically sorted, and therefore supports an efficient longest-path algorithm. Each longest path computation takes $O(|V(G_c^m)| + |E(G_c^m)|)$ time, the same runtime as constructing the model computation graph G_c^m itself.

Using the absolute value of our attribution scores as weights, we initialize our circuit with the longest path from any input to each model output. Then, continuing down the top-k edges which have not yet been included, we compute the longest path containing that edge and add it to the circuit. Thus once scores are computed, finding a circuit that includes the top k edges takes time $O((k+d^L)(|V(G_c^m)|+|E(G_c^m)|))$, where d^L is the output dimension. This way, MINAR guarantees that the identified circuit is a connected subgraph of the computation graph whose only parentless and childless nodes are the model inputs and outputs, respectively.

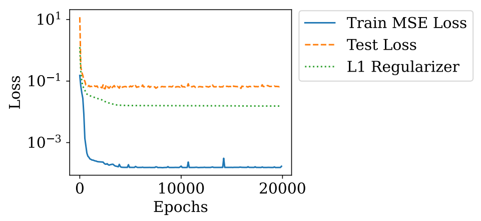
5 Results

We demonstrate our circuit discovery method using two classical algorithmic tasks in the neural algorithmic reasoning literature: single-source shortest paths (via Bellman-Ford) and node reachability (via breadth-first search). We test first shortest paths by itself, then test shortest paths and reachability in parallel, as in [16]. In the shortest path task, we validate our method by identifying the circuit predicted by Nerem et al. [10] to implement the Bellman-Ford algorithm. For the parallel task, we examine the hypothesis of Veličković et al. [16] that a model predicting shortest path distance and reachability in parallel may experience some amount of transfer between tasks, reusing part of the computation for one task to perform the other.

Both tasks share the same training set, constructed as in [10], but with additional node features and labels to support the reachability task. Specifically, each node is given two initial features based on the typical initialization for Bellman-Ford and breadth-first-search:

$$x_v^{\text{SP}} = \begin{cases} 0 & v \text{ is the source} \\ B & \text{otherwise.} \end{cases} \quad \text{and} \quad x_v^{\text{BFS}} = \begin{cases} 1 & v \text{ is the source} \\ 0 & \text{otherwise.} \end{cases} \tag{6}$$

Here B is any large number greater than any path length, which we take to be $B = 1000$. For the shortest path GNN, only x_v^{SP} is provided as input to the model. When the two tasks are performed in parallel, the initial node feature is the concatenation $(x_v^{\text{SP}}, x_v^{\text{BFS}})$. For the test set, we additionally include a number of balanced tree graphs to provide more graphs with unreachable nodes. We discuss



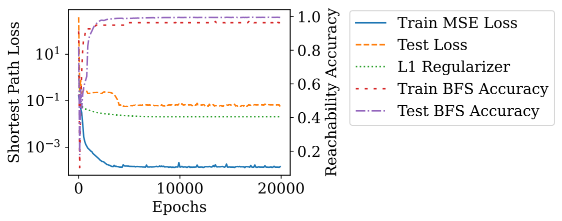


Figure 1: MSE training loss, multiplicative test loss, and L_1 regularization term for Bellman-Ford MinAggGNN (left) and parallel Bellman-Ford and BFS MinAggGNN (right). The right plot also shows train and test accuracy on the BFS reachability task.

the dataset in greater detail in Appendix B. In our circuit discovery experiments, we corrupt the input data by setting every edge weight to zero and flipping the input features:

$$x_v^{\mathrm{SP}\prime} = \begin{cases} B & v \text{ is the source} \\ 0 & \text{otherwise} \end{cases} \quad \text{and} \quad x_v^{\mathrm{BFS}\prime} = \begin{cases} 0 & v \text{ is the source} \\ 1 & \text{otherwise.} \end{cases} \tag{7}$$

We also perturb the edge weights, setting them to zero in the corrupted data. In both experiments, we evaluate the identified circuits by performing inference using just the circuit components. We achieve this by zeroing out network parameters that are not included in the identified circuit and performing a forward pass with the ablated network.

5.1 Bellman-Ford

We validate MINAR by replicating [10]. We train a minimum-aggregated message-passing network (which [10] dubs a MinAggGNN) to predict single-source shortest path distances. We use a two-layer network, corresponding to two steps of Bellman-Ford. Each layer is given by

$$\Phi_v^{(\ell+1)} = f_{\mathrm{Up}}^{(\ell)}\left(\Phi_v^{(\ell)}, \min_{(u,v)\in E(G)} f_{\mathrm{Agg}}^{(\ell)}(\Phi_u^{(\ell)}, e_{u,v})\right) \tag{8}$$

where we implement $f_{\mathrm{Agg}}^{(\ell)}$ and $f_{\mathrm{Up}}^{(\ell)}$ as two-layer MLPs and we use the minimum operation as the aggregator to mimic the Bellman-Ford algorithm. By training with L_1 sparsity regularization and a small curated training set, [10] shows that such a GNN must implement the Bellman-Ford algorithm. While we use MSE during training, we follow [10] in evaluating using a percentage-based test loss:

$$L_{\text{test}} = \frac{1}{|\mathcal{G}_{\text{test}}|} \sum_{G\in\mathcal{G}_{\text{test}}} \sum_{v\in G \text{ reachable}} \left|1 - \frac{y_v}{\Phi(v)}\right| \tag{9}$$

where N is the number of reachable nodes from the source of each graph and y_v is the true label for each reachable node. The trained GNN reaches an MSE of $L_{\mathrm{MSE}} = 0.0002$ and a test loss of $L_{\text{test}} = 0.0673$. We plot the loss and the L_1 regularization term in Figure 1, showing that the model has converged to a sparse, generalizable solution.

Having trained a model to implement a shortest-path solution, we use EAP-IG with $m = 20$ steps to identify the responsible circuit (Figure 2). The resulting circuit consists of only 17 edges out of 18240 edges in the full computation graph. For comparison, a minimum of 10 parameters are predicted by [10]. The circuit, taken as a subnetwork of the full model, achieves a loss of 0.0644 on the test set, matching the high performance of the full model. In fact, the circuit achieves a slightly lower loss overall, although not substantially. In this example, MINAR successfully recovers a small circuit that captures the behavior of the full model, validating our approach.

5.2 Bellman-Ford and breadth-first search in parallel

We expand the Bellman-Ford example by introducing a second task: predicting reachability by breadth-first search. As with Bellman-Ford, the model's two layers correspond to two steps of BFS. The combination of Bellman-Ford with BFS was investigated by Veličković et al. [16], who note that both algorithms traverse a graph in the same manner, and hence hypothesize that learning one task can benefit performance on the other.

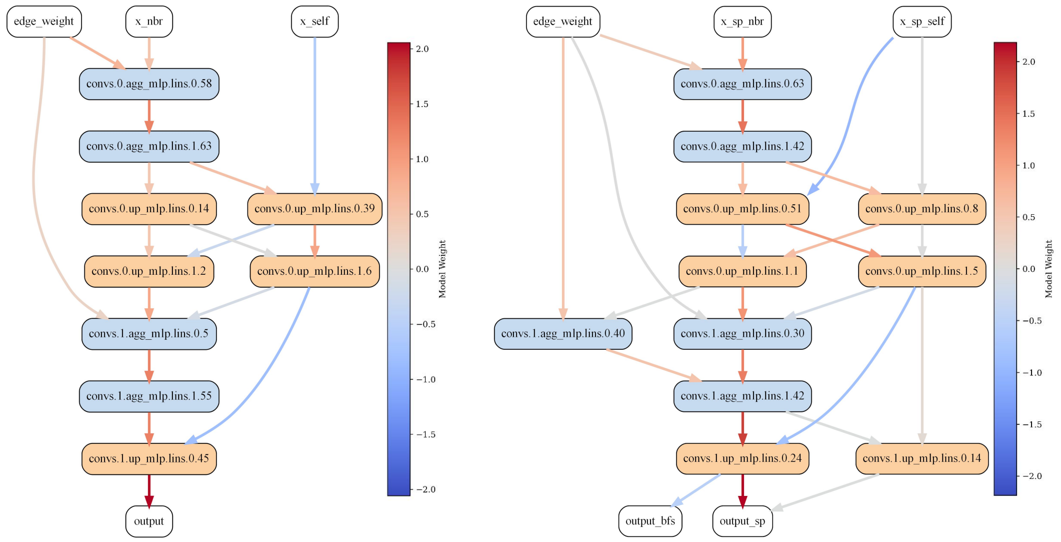


Figure 2: Identified circuits in the Bellman-Ford MinAggGNN (left) and parallel Bellman-Ford with BFS MinAggGNN (right). Nodes are individual MinAggGNN neurons. Input and output neurons are colored white, f_{Agg} neurons are colored blue, and f_{Up} neurons are colored orange. Circuit edges are colored by corresponding model weights.

We train simultaneously, using MSE for the shortest path task and binary cross-entropy for the reachability task. Because we use the same training and testing sets as the Bellman-Ford experiment, the positive and negative reachability classes are imbalanced. (About 91.24% of training nodes and 81.98% of test nodes are reachable.) Therefore, we use class weighting so that the positive and negative classes have equal weight during training. We additionally scale the BCE loss by a factor of 25 during training, as we observed that the MSE and L_1 terms dominated training otherwise. Figure 1 shows the loss and accuracy curves of the model during training, with a test loss of 0.0604 on shortest path and a test accuracy of 0.9943 on reachability. We again use EAP-IG with $m = 20$ steps to identify the circuit (Figure 2). We identify a circuit with 25 edges (out of 18432) which achieves a test loss of 0.0635 on shortest paths and a reachability accuracy of 0.9664.

Examining the circuit for the parallel GNN in Figure 2, we notice the nodes `x_sp_nbr` and `x_sp_self` correspond to the shortest path input feature. The BFS feature is absent, indicating that the model does not actually use the BFS feature x^{BFS}. Instead, the model simply recycles steps from the shortest path computation: comparing the two circuits in Figure 2 reveals that the Bellman-Ford computation follows a very similar structure in both models. However, in the final layers of the parallel model, the same neuron `convs.1.up_mlp.lins.0.24` is responsible for the bulk of both outputs. Thus we see that rather than fully implement BFS and Bellman-Ford in parallel, the parallel GNN uses a heuristic from the shortest path calculation to perform the reachability prediction.

6 Conclusion

We propose MINAR, bringing methods from mechanistic interpretability to the setting of neural algorithmic reasoning with graph neural networks. To our knowledge, our work is the first to attempt circuit discovery in GNNs to study NAR. Through two case studies, we demonstrate how MINAR can be used to identify circuits implementing Bellman-Ford and BFS in trained GNNs, two classical tasks in NAR. We chose these settings because the learned algorithms are well-understood and clearly interpretable, allowing us to validate our method. In future work, we intend to apply MINAR to novel algorithmic and mathematical tasks or to algorithmically-aligned tasks that use real data containing high-dimensional features.

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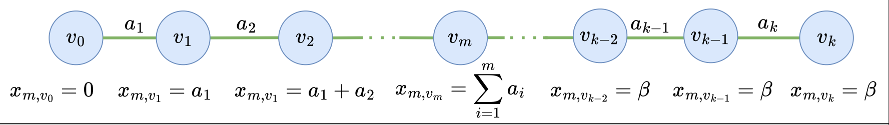
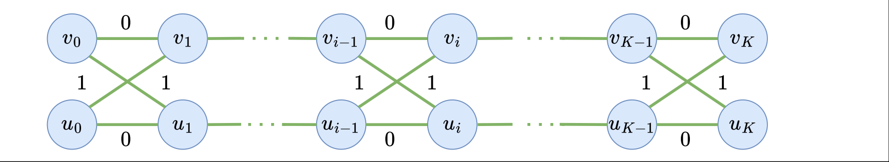
$P_k^{(m)}(a_1, \dots, a_k)$	
$H_K^{(0)}$	

Figure 3: Training graphs for the Bellman-Ford MinAggGNN from [10].

A Model Training

We perform our computations on an NVIDIA RTX A6000 Laptop GPU using PyTorch [12] and PyTorch-Geometric [4]. For each MinAggGNN, $f_{\text{Agg}}^{(\ell)}$ and $f_{\text{Up}}^{(\ell)}$ are implemented as two-layer MLPs with a hidden dimension of 64. The intermediate dimension of each network is 8. We train each model using AdamW [8] with a learning rate of $\gamma = 0.001$ for 20,000 epochs using full batches and an L_1 regularization term of $\eta = 0.001$.

B Training Data

Following [10], we construct a training set $\mathcal{G}_{\text{train}}$ from the graphs depicted in Figure 3 for $K = 2$. It includes all path graphs of the form $P_{K+1}^{(1)}(a, \dots, b, \dots, 0)$ for $a, b \in \{0, 1, \dots, 2K\} \times \{0, \dots, 2K + 1\}$ (where b is the weight of the K-th edge). It also includes the graph $H_K^{(0)}$ from Figure 3 and the special path graphs $P_1^{(0)}(1)$, $P_2^{(1)}(1, 0)$. We also include extra path graphs: four three-node path graphs initialized at step zero of Bellman-Ford and four four-node path graphs initialized at step two of Bellman-Ford, each with randomly generated edge weights.

For the test set, we also largely follow [10]. We include a collection of 3, 4, and 5-node cycle graphs; complete graphs on 5 to 200 nodes; and Erdős-Rényi graphs on 5 to 200 nodes with $p = 0.5$. To provide extra examples of graphs with unreachable nodes, we also generate binary and ternary trees of depths of 3 and 4. All test graphs have randomly generated edge weights, and the test set contains 300 graphs in total.

C Regularization

Our use of an L_1 sparsity regularization follows Nerem et al. [10], who show that training their MinAgg GNN with L_1 regularization is necessary to induce the desired Bellman-Ford implementation. Regularization is also employed in several mechanistic interpretability works to induce a “correct” implementation in a trained model. For example, Zhong et al. [21] use weight decay when training their model to perform modular addition, and Li et al. [7] show that weight decay is necessary to prune “vestigial” circuits that implement trivial heuristics early in training. The impact of regularization can be seen in the parameter summaries for the trained networks, as shown in Figure 4 and Figure 5.

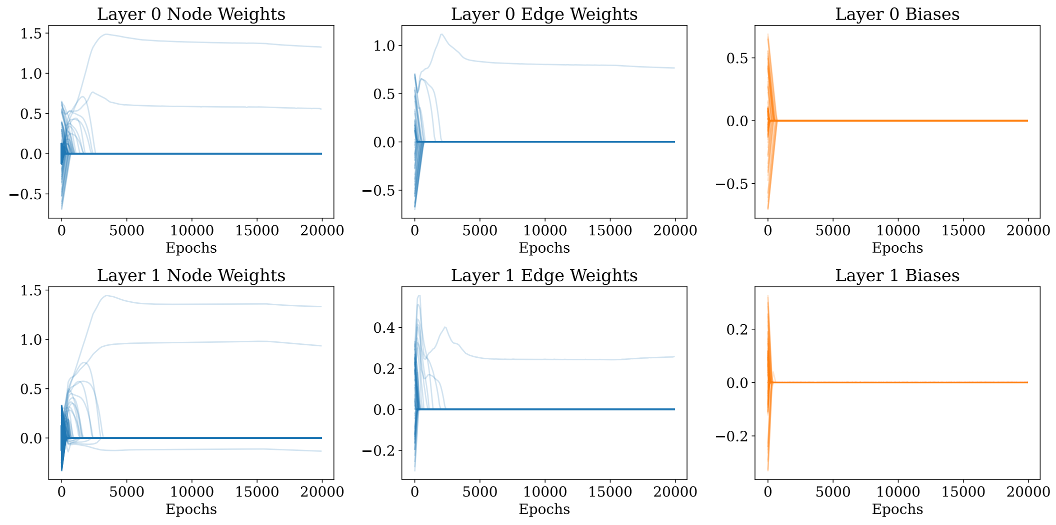


Figure 4: Parameter summaries for each component of the Bellman-Ford MinAggGNN.

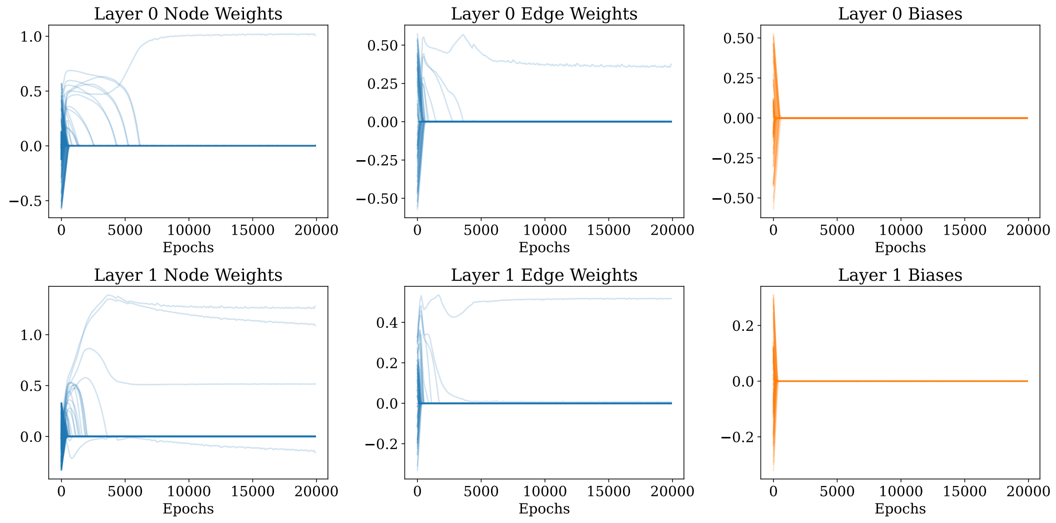


Figure 5: Parameter summaries for each component of the parallel Bellman-Ford and breadth-first search MinAggGNN.

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