Design of a CMOS FD-NIRS System With Fully Integrated Analog Front-End and Readout

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Abstract—An integrated, dual-channel, Frequency Domain Near Infrared Spectroscopy system with integrated laser driver, analog front-end, phase and amplitude detection is designed in 180nm XFAB PDK. The system can accommodate both multi-distance and Dual Slope methods. The channels were designed to have 145-MHz bandwidth with 8 picofarad photodetector junction capacitance, provide ~115dB gain with 56 dB dynamic range and measure the phase difference between channels with 0.02° resolution.

Index Terms—Frequency domain near infrared spectroscopy, analog front-end, transimpedance amplifier, amplitude detection, phase detection, heterodyne

I. INTRODUCTION

Near-infrared spectroscopy (NIRS) is a non-invasive optical technique that can be used to characterize the optical properties of highly scattering media by illuminating it with light at one point and detecting the reflected or transmitted light at a nearby location, typically a few centimeters from the source [1]. In biomedical context, 650-900 nm wavelengths are chosen due to low water absorption in tissue within this optical window [2]. Although many chromophores such as water, lipid, melanin [3], and bilirubin still contribute to light absorption in this spectral range, oxyhemoglobin (HbO₂) and deoxyhemoglobin (HbR) predominantly determine the absorption coefficient (μ_a) , making it possible to estimate their concentrations from μ_a measurements [4]. As a result, NIRS has found extensive use in clinical studies, including applications in pediatrics [5], breast cancer [6], functional brain imaging [1], [7], neonatal care [8], ischemia [9], ulcers [10], and peripheral artery disease [11]. One example of sensor placement can be seen in Fig. 1.

NIRS techniques can be categorized into three main types: continuous-wave (CW-NIRS) [12], time-domain (TD-NIRS) [13], and frequency-domain (FD-NIRS) [7], which differ primarily in their use and type of light source modulation. The simplest form, CW-NIRS, uses an unmodulated light source to provide constant illumination. Changes in detected intensity over time reflect variations in absorption ($\Delta \mu_a$) due to hemodynamic or other physiological events, but the absolute values of μ_a and μ_s' can't be measured without some assumptions.

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In contrast to CW-NIRS, the other two methods employ a modulated light source. In TD-NIRS, this modulation takes the form of ultra-short pulses on the order of picoseconds, while in FD-NIRS, light is modulated sinusoidally at radio frequencies (\sim 50–1000MHz). This time-dependent modulation allows the light intensity to be analyzed as a function of time, enabling the calculation of the mean photon transit time through the medium. These additional temporal measurements provide the necessary information to recover the absolute values of μ_a and μ'_a .

For TD-NIRS, commercially available picosecond laser sources are typically expensive and bulky. Moreover, resolving the detected light requires high-speed photodetectors. In contrast, FD-NIRS systems involve less hardware complexity, therefore they can be constructed using standard laser diodes and readily available photodetectors.

Frequency-domain NIRS systems have previously been implemented using different configurations, some rely on commercial vector network analyzers (VNAs) to retrieve intensity and phase data [14], [15], while others use direct sampling with high-speed ADCs connected directly to high-frequency signals [16]–[18]. In addition to direct sampling, other strategies include homodyne detection, where signals are mixed with a same-frequency local oscillator and processed using I-Q demodulation [19]–[21], and heterodyne detection [22]–[25], which uses a slightly offset local oscillator to shift the signals to lower frequencies, simplifying subsequent sampling.

Although all of these methods have proven to be effective, only some are suitable for integrated circuit (IC) implementation. Nonetheless, integrated approaches have emerged that show significant potential towards wearability and portability [26]–[28]. We chose the heterodyne approach specifically for its compatibility with integrated circuit design and have previously reported multiple iterations of systems at various levels of integration [29]–[37]. In this work, we present the latest iteration of our design, where we integrated the laser driver circuit, phase detector, and amplitude detector, getting close to a single-IC FD-NIRS solution.

II. SYSTEM ARCHITECTURE

We can recognize several key tasks that a heterodyned FDNIRS system must accomplish: it needs to amplify a

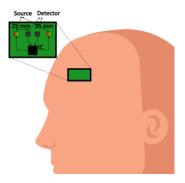


Fig. 1. An example of sensor placement for brain neural measurements

faint (on the order of nanowatts, nW) but high-frequency (~50–1000 MHz) optical signal, down-convert this signal to a lower frequency, and accurately measure its amplitude and phase relative to a reference signal. In designing such a system, critical performance metrics that strongly influence the requirements of the system are noise, bandwidth, and dynamic range. Given the level of the expected signal, noise performance is crucial. Sufficient bandwidth is needed since higher operating frequencies improve phase contrast. Finally, a high dynamic range is essential, as signal levels can vary by up to a factor of 20 depending on the source–detector separation in FDNIRS measurements.

In this work, the system has two identical analog frontend chains that consists of a fully differential transimpedance amplifier (TIA) followed by a mixer for down conversion and then an instrumentation amplifier. After that, the amplitude and phase detector circuits measure the amplitudes and the phase difference between these two channels. The phase detector's output is a 14-bit digital signal, and the amplitude detectors'

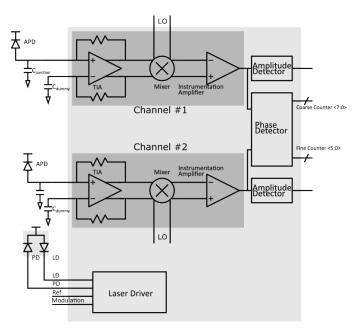


Fig. 2. The block diagram of the proposed system

outputs are analog signals. On top of the two receiver chains, the laser driver circuit is also included. The system block diagram can be seen in Fig.2.

A. Analog Front-End

The TIAs are the first circuit that interfaces with the APDs, therefore their noise performance is critical, as their noise dominates the rest of the channel. Other important metrics for the TIA design were bandwidth and dynamic range. Keeping all these constraints in mind, the architecture chosen for the TIAs were the fully differential resistive feedback architecture, with the core amplifier being distributed into 3 separate amplifiers, for extended bandwidth. The feedback resistors are $100~\mathrm{k}\Omega$, providing $100~\mathrm{d}B$ gain, with integrated input referred noise of $\sim \! 30~\mathrm{n}A_{rms}$ and dynamic range of $\sim \! 56~\mathrm{d}B$.

The outputs of these TIAs are then down-converted with a pair of mixers. These mixers were designed as double balanced Gilbert Cell Mixers, with the input stage being implemented as Folded Cascode. Resistive degeneration in the folded input stage was also used to improve the linearity of the mixer, since the dynamic range and linearity of the system was recognized as one of the critical metrics [37]. The mixers in this design can provide a maximum of 14 dB of conversion gain, which can be adjusted with the LO power, and have dynamic range of ~41 dB at the LO power that gives the maximum gain.

A rail-to-rail instrumentation amplifier follows the mixer. It turns the differential output of the mixer into single ended, adjusts the common mode and also acts as a buffer to isolate the analog front end and the subsequent amplitude and phase detectors. The analog front-end was estimated to consume 5.4 mA current or 11.4 mW power per channel.

B. Amplitude Detector

The amplitude detector circuit works as a peak detector and is based on [38]. It consists of an Op Amp, a cascode current mirror, a capacitor to hold the output voltage and one transistor for resetting, and can be seen in Fig.3.

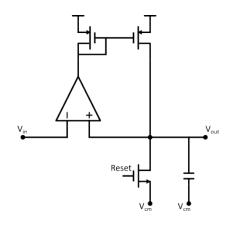


Fig. 3. The peak detector based amplitude detector

Assuming a sine wave input, as the input voltage increases and goes above the output voltage, the output of the OPAMP goes low and starts sinking current from the left hand side

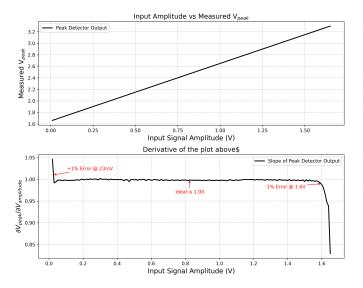


Fig. 4. (a) The input amplitude vs output characteristic of the amplitude detector. (b) the DNL of the amplitude detector

of the current mirror, which is then copied to the right hand side and charges the capacitor, and hence the output voltage tracks the input. Then as the input voltage starts going below the output, the OPAMP stops sinking current. Since there's no current to be copied, the output stops charging. The output is held at the peak level until the Reset signal comes, which discharges the output to $V_{\rm cm}$. Since the OPAMP is rail-to-rail, the amplitude detector works all the way up to $V_{\rm DD}$. In Fig.4, the differential nonlinearity (DNL) of the amplitude detector can be seen. The error on the amplitude detector is less than 1% from ${\sim}20$ mV to ${\sim}1.6$ V. Similarly, Fig.5 shows the transient response of the amplitude detector with input amplitudes ranging from 100 mV to 1.6V.

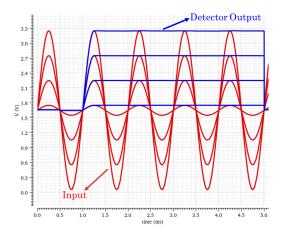


Fig. 5. The transient response of the amplitude detector different input amplitudes

C. Phase Detector

The phase detector was designed in a Coarse-Fine Detection scheme, where one of the two 7-bit Coarse Detectors (namely

I and Q counters) works by counting an external clock inbetween the zero-crossing instances of the two channels. The Q counter works when the phase difference between the circuits is between 0° and 180°, and the I counter works when the phase different is between 180° and 360° (Fig. 6). The 8th bit represents which one of these 7-bit Coarse Detector have been the active one. An earlier version of this can be found in [38]. The zero-crossing instances of each channel are sensed with Positive Feedback Amplifier based comparator circuits, then the outputs of the comparators are used to drive a couple of Up-Down Counters. The counters are designed in a way that they count Up/Down only if either of the signals have had a zero-crossing event. When both signals cross, the counters stops. The clock speed was chosen as 2.56 MHz for a downconverted signal of 10 kHz. The 8-bit Coarse Counter with 2.56 MHz clock speed with 10 kHz down-converted signal is designed to give a phase resolution of $\sim 1.40^{\circ}$ by itself.

	Priase Sweep Example			
င်္ခ Coarse Q Counter	<i>IIIIIIIIX</i> X	128(0)		
မို့ (Coarse Q Counter	0		32	
င္တဲ့ Coarse Q Counter	0	X///X	64	
ဗိုင် Coarse Q Counter	0	X/////X	96	
© Coarse Q Counter	0 /	<i> </i>	128(0)	
Coarse I Counter	0		32	
Coarse I Counter	0 \(///)		64	
Coarse I Counter	0 ///////	96		
င္တြင္ Coarse I Counter	//////////////////////////////////////	128(0)		

Fig. 6. The coarse counter results when the phase difference between the two channels swept from 0° to 360°

The 6-bit Fine Counter (Fig.7) is based on a delay line approach, where each delay element introduces \sim 6.2 ns time delay, with a total of 64 elements in series. The Fine Counter is triggered when one of the signals has a zero-crossing event. This trigger signal propagates the delay line one element at a time until the Coarse Counter is triggered. The output of the Fine Counter is in thermometer code format which is converted to binary to reduce the number of bits and pins required.

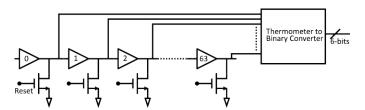


Fig. 7. The fine counter delay line with the thermometer to binary converter

The delay elements are designed as two current-starved inverters, where the current is supplied from outside, hence controllable and fine tunable to achieve the desired delay time.

The delay time is tuned so that all 64 elements fit into one Coarse Count. This approach, combined with the 8-bit Coarse Counter, divides one period of the down-converted signal into 64*256 = 16384 steps. Assuming a down-converted signal of 10 kHz and Coarse Counter clock of 2.56 MHz, we can achieve a 0.022° phase resolution. To reiterate the advantage of the this approach, if we wanted to achieve the same phase resolution by only counting clocks between the zero-crossing events, we would need a clock speed of about 163 MHz.

D. Laser Driver

The Laser Driver circuit (Fig.8) is based on the popular linear current regulator topology, but one key improvement to keep the optical power output stable. The laser diodes we use in our work (HL6750MG and HL8338MG, Thorlabs) come with an integrated photodiode that generates a current that is proportional to the optical power output of the laser diode. In our laser driver circuit, we direct this current through a resistor to produce a voltage, and use this voltage as the non-inverting input of the OPAMP. The feedback loop forces OPAMP's inputs to be equal, which means constant feedback current coming out of the integrated photodiode. This approach ensures the same optical power from the laser diodes over temperature, aging etc. The sine wave modulation is being provided from a separate Direct Digital Synthesizer from outside. A double pole double throw (DPDT) switch can be used to switch between two laser diodes.

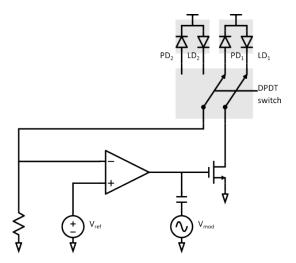


Fig. 8. Laser driver circuit with reference current feedback

III. CONCLUSION

In this work, an integrated FD-NIRS system with analog front end, laser driver, phase and amplitude detectors has been presented. The design was done in 180nm IBM PDK. The analog front end achieved ~ 115 dB gain, 30 nA_{rms} integrated input referred noise current, 145 MHz bandwidth and ~ 56 dB dynamic range, with power consumption of 11.4 mW per channel. The amplitude detector works up to the supply voltage thanks to rail-to-rail operation and the phase detector

achieves 0.022° for 10 kHz signals, or \sim 6.2 ns resolution with a clock speed of 2.56 MHz. This iteration of our work constitutes a significant step in our efforts to create a fully integrated and wearable FD-NIRS platform.

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