Maximizing Parallelism in Distributed Training for Huge Neural Networks

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Abstract

The recent Natural Language Processing techniques have been refreshing the stateof-the-art performance at an incredible speed. Training huge language models is therefore an imperative demand in both industry and academy. However, the huge models impose challenges to both hardware and software. Graphical processing units (GPUs) are iterated frequently to meet the exploding demand, and a variety of ASICs like TPUs are spawned. However, there is still a tension between the fast growth of the extremely huge models and fact that Moore's law is approaching the end. To this end, many model parallelism techniques are proposed to distribute the model parameters to multiple devices, so as to alleviate the tension on both memory and computation. Our work is the first to introduce a 3-dimensional model parallelism for expediting huge language models. By reaching a perfect load balance, our approach presents smaller memory and communication cost than existing state-of-the-art 1-D and 2-D model parallelism. Our experiments on 64 TACC's V100 GPUs show that our 3-D parallelism outperforms the 1-D and 2-D parallelism with 2.32X and 1.57X speedup, respectively.

1 Introduction

To deal with the growing amount of data, nowadays people are squeezing the computation from GPUs or FPGAs to get larger and more powerful neural networks. Consequently, records are being broken in a variety of Natural Language Processing (NLP) tasks ranging from classification, question answering to translation as the language models are becoming much deeper. In the meantime, starting from the emergence of Transformer models [20] like BERT [4], the trend to increase model sizes becomes even more radical. Since then, the Moore's Law can never reach the growth of language models. Past several years have witnessed the creation of gigantic models, like GPT-2 [13] and GPT-3 [2], which are able to compose texts and synthesize images. The amazing performance is also attracting attention from industry. Google recently announced its Multitask Unified Model (MUM) for language understanding, LaMDA for conversation, and TPUv4 chips for model training.

The surging model size brings challenges in terms of both memory and computation. Apart from developing chips such as GPU and TPU with higher computation capability and memory limit, activation checkpointing techniques are developed to squeeze a large model into a single device

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that would otherwise not be able to host such a big model. Moreover, ZeRO-infinity techniques [14, 14, 15] are proposed to utilize the memory of CPU or other memory device external to GPU without sacrificing the data transmission time. Data parallelism is a dominant practice to fully utilize available HPC resources. It distributes a large minibatch to multiple devices, where each device holds an identical model replica, and finally gathers the gradients for synchronous parameter update. With recent optimization techniques [6, 22, 23, 24], it is now able to train very large minibatches on thousands of GPU devices.

Another branch is model parallelism, the main idea of which is to divide both computation and memory of a single neural network to multiple devices. Pipelined parallelism [7, 9] is proposed to split the whole model by layer, which will be executed in a pipeline fashion. Mixed precision training is utilized to reduce both memory and computation cost. Megatron-LM [17] integrates both model parallelism and data parallelism by splitting the parameter tensor among model parallel groups, achieving the state-of-the-art language model. Recently, a 2-dimensional matrix-matrix multiplication algorithm has been introduced into language model training [21], thus bridging the gap between traditional high-performance computing and machine learning. In this work, we stride a step forward and propose a 3-D model parallelism technique to further harness the capability of GPU clusters. We list our main contributions as follows.

- We propose a 3-D model parallelism algorithm for linear operations, which can reach a perfect load balance, so as to provide the optimal efficiency;
- We use our 3-D model parallelism to implement an efficient Transformer model based on the existing PyTorch Transformer implementation and distributed communication package;
- We demonstrate the effectiveness of our 3-D model parallelism on 64 GPUs by comparing it with the existing 1-D and 2-D approaches. The results present the superiority of our 3-D parallelism with 2.32X and 1.57X speedup, respectively.

2 Background

2.1 Transformer Language Models

There has been a recent trend to use pretrained language models to help people train specific natural language processing (NLP) tasks, as pretrained models leverage the understanding of very large corpus (e.g. Wikipedia) to alleviate the efforts of training entire language models. Transformer is one of the current dominant choices of pretraining language models, achieving the state-of-the-art compute efficiency and prediction accuracy. The Transformer language model uses deep attention modules to transform a given sequential input into another sequential output. Like LSTM, a complete Transformer model includes two parts, an Encoder and a Decoder, but each consists of attention layers rather than recurrent layers. However, recent state-of-the-art Transformer applications, such as BERT [4], GPT-2 [13], and GPT-3 [2], adopt more concise structures that only use necessary Encoders or Decoders on demand.

Nevertheless, training Transformer language models can be extremely computational expensive. The recent language models advance their accuracy with a rising number of parameters (e.g. OpenAI GPT: 110M [12]; BERT: 340M [4]; GPT-2: 1.5B [13]; GPT-3: 175B [2]; Switch Transformers: 1.6T [5]). In the meantime, to deal with huge language corpus, there has been a growing interest in using large minibatches to reduce training time. Therefore, efficient systems to expedite Transformers become an urgent demand for training large language models.

2.2 Data and Model Parallelism

Data parallelism is the most common paradigm to parallel the computation of deep neural networks. This approach distributes the entire minibatch across multiple workers, which execute a single replica of the model and communicate with each other for synchronization at the end of each training step. It is easy to use more devices to train larger minibatches. By taking advantage of recent optimization techniques [18, 22, 23, 24, 11], training speed reaches almost linear scaling with the number of devices. However, due to the issue of generalization gap [10, 8], using very large minibatches requires extra efforts to guarantee the convergence performance [6, 22, 23, 24]. Besides, a practical limitation

is that large Transformer models that have more than billions of parameters are basically not able to be accommodated into the memory of a single GPU device.

Model parallelism can successfully remove the above memory limitation. There are two model parallel paradigms. First, the layer-wise pipelined parallelism splits the entire model by layer, and execute the layers in the pipeline fashion. Some approaches [7, 9] use their algorithms to tackle the inconsistency issue among different pipelines, so that the computation and communication time can be overlapped. However, since each training step requires both forward and backward processing, there will be an inevitable bubble overhead, so that the compute resources cannot be fully utilized.

The second model parallel paradigm is the intra-layer parallelism, which is orthogonal to the pipelined parallelism. It distributes the operations in each layer such as matrix multiplications and activations across multiple workers. For example, Mesh-Tensorflow [16], a framework proposed by Google, provides a convenient way for users to allocate the partition of tensor dimensions. Then the matrix multiplications can be automatically partitioned in a single dimension and distributed to workers, without any user elaboration. Similarly, Megatron-LM [17] adopts a 1-D matrix partition strategy to implement the Transformer model. It splits matrices along rows or columns, and gathers results with the all-reduce operation. Moreover, Optimus uses the Scalable Universal Matrix Multiplication Algorithm (SUMMA) [19], a 2-D parallel strategy for matrix multiplications, which helps to reduce memory and communication costs required for executing the Transfer model. Our approach aims to take a step further and use the 3-D parallelism to improve the performance by optimally balancing the computation, memory and communication load.

2.3 3-D Parallel Matrix Multiplication

In this section, we provide an outline of the 3-D parallel matrix multiplication algorithm [1], which is adopted in our approach.



Figure 1: The structure of a 3-D processing cube with $P = p^3$ processors. The colored block (i, j, k) represents an example of a single processor.

This algorithm computes the multiplication between two dense matrices concurrently on $P = p^3$ processors, as illustrated in Figure 1, where P processors can be stacked into a p^3 cube. In this cube, let A, B, C denote the planes, x, y, z denote the directions for the planes, and i, j, l denote the different indices along the directions. We also use A, B, C to represent the matrices involved in the multiplication, so that $A_{ij}, 0 \le i, j < p$ is supposed to represent a submatrix of A.

For simplicity, we consider an example of the 3-D matrix multiplication C = AB on a $2 \times 2 \times 2$ processing cube. We split A and B of size (M, N) and (N, K) into 2×2 partitions as follows, so that the sizes of each partition A_{il} and B_{lj} is (M/2, N/2) and (N/2, K/2) respectively, for $0 \le i, j < 2$.

$$A = \begin{bmatrix} A_{00} & A_{01} \\ A_{10} & A_{11} \end{bmatrix}, \quad B = \begin{bmatrix} B_{00} & B_{01} \\ B_{10} & B_{11} \end{bmatrix}.$$
 (1)



Figure 2: An example of the 3-D parallel matrix multiplication of size $2 \times 2 \times 2$.

Each partition A_{il} is stored in the processor (i, 0, l), while B_{lj} is stored in (0, j, l). Before multiplication, we first broadcast each A_{il} from (i, 0, l) along the y direction (Figure 2a), so that we have A_il on each (i, j, l). Similarly, we broadcast each B_{lj} along the x direction (Figure 2b). Next, we can compute $C_{ijl} = A_{il}B_{lj}$ on each processor (i, j, l). Then we reduce C_{ijl} to (i, j, 0) along the z direction to derive $C_{ij} = \sum_l A_{il}B_{lj}$ (Figure 2c). Thus, we finally get C = AB as

$$C = \begin{bmatrix} A_{00}B_{00} + A_{01}B_{10} & A_{00}B_{01} + A_{01}B_{11} \\ A_{10}B_{00} + A_{11}B_{10} & A_{10}B_{01} + A_{11}B_{11} \end{bmatrix}.$$
 (2)

3 3-D Parallel Transformers

We now describe our main design and implementation of the 3-D parallel Transformer language model.

3.1 3-D Operations

As demonstrated in Figure 3, the Transformer language model computes its hidden states from top to bottom, through multiple Transformer blocks. In each block, the major computation in both the Self-Attention and Multi-Layer Perception (MLP) layer involves linear operations and activations. While activation operations can be independently executed in parallel, to accelerate linear operations is the key to reduce execution time of the Transformer model. We firstly tackle the load balancing issue of the original 3-D matrix multiplication, and then present the designs of both 3-D parallel matrix-matrix and matrix-vector operations that are used in the Transformer model.

3.1.1 Load Balancing

We consider the matrix multiplication C = AB between the input matrix A of size (M, N) and the weight matrix B of size (N, K) on $P = p^3$ processors, which requires MNK calculations in total. An intuitive way to store the matrices is to partition each dimension of the matrices by p, and hold each partition A_{il} on the processor (i, 0, l), B_{lj} on (0, j, l), and C_{ij} on (i, j, 0) respectively. In this way, we will need to broadcast each partition A_{il} and B_{lj} across at least p processors before multiplication, and then reduce the partitions C_{ij} after the multiplication, so as to guarantee the consistency among them. Therefore, an obvious issue is that the storage is imbalanced, so that we waste a great amount of redundant memory in the processor (i, j, l) if $i \neq 0$ or $j \neq 0$ or $l \neq 0$. In the meantime, the imbalanced storage will result in imbalanced activation or element-wise operations, causing the inefficiency that the computation of such operations is not evenly distributed to all processors.

To eliminate the redundancy caused by the gap between the number of computation and memory dimensions, our insight is to distribute the matrices evenly to the cube. More specifically, we define $m = M/p^2$, $n = N/p^2$, $k = K/p^2$. Let each processor (i, j, l) hold the partitions $A_{ijl} = A[imp + jm : imp + jm + m - 1, lnp : lnp + np - 1]$, $B_{lji} = B[lnp : lnp + np - 1, jkp + ik : jkp + ik + k - 1]$, as shown in Figure 4a. Before the multiplication, instead of the original broadcast operation, we use an all-gather operation along the y direction to copy $A_{il} = A[imp + mp - 1, lnp : lnp + np - 1]$ across processors (i, j, l) for $0 \le j < p$ (Figure 4b). Similarly,





(a) The input and weight (b) All-gather A_{il} in the y submatrices on each pro-direction.



Figure 3: Architecture of the Transformer model that consists of multiple Transformer layers.

(c) All-gather B_{lj} in the x (d) Compute each C_{ijl} and direction. z direction.

Figure 4: Load-balanced 3-D matrix-matrix multiplication.

we execute an all-gather for $B_{lj} = B[lnp : np - 1, jkp : jkp + kp - 1]$ (Figure 4c). Then we compute $A_{il}B_{lj}$ on each processor, and use a reduce-scatter operation in the z direction to get $C_{ij} = \sum_{l} A_{il}B_{lj}$ across processors (i, j, l) for $0 \le l < p$. Thus, we will finally get $C_{ilj} = C_{ij}[lm : lm + m - 1, :] = C[imp + lm : imp + lm + m - 1, jkp : jkp + kp - 1]$ in each processor (i, j, l), as shown in Figure 4d. In overall, the memory cost per processor of our approach is supposed to be $(M/p^2) * (N/p) + (N/p) * (K/p^2) + (M/p^2) * (K/p) \approx O(1/p^3) = O(1/P)$.

For vector parameters that are used in matrix-vector operations, we store the vector b of size N diagonally on the B plane, i.e. only the processors (i, j, l) holds $b_{ji} = b[jnp+in: jnp+in+n-1]$ for $j = l, 0 \le i, j, l < p$, as shown by the colored blocks in Figure 5. To execute a matrix-vector operation, e.g. A + b, we need to broadcast b_{li} in the y direction, and then get b_l by all-gathering them in the x direction. In contrast, to execute C + b, we need to broadcast b_{ji} in the z direction before all-gathering them. Then we can get $A_{il} + b_l$ or $C_{ij} + b_j$ on each processor.



Figure 5: Balancing vector parameters for matrix-vector operations.

We need to notice that the communication directions of the input matrix A and output matrix C are different. To execute the Transformer model, since the output states of each linear layer are basically the input states of the next layer, we exchange the communication directions y and z for the input and output states after the 3-D parallel matrix multiplication, while keep the direction x for the network weights. The matrix-vector operations are supposed to have no affect on the communication directions.

3.1.2 Matrix-matrix Operations

In the Transformer model, three forms of matrix-matrix multiplication, including C = AB, $C = AB^T$ and $C = A^T B$, are involved w.r.t the following differentiation formulas.

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$$C = AB, \dot{A} = \dot{C}B^T, \dot{B} = A^T\dot{C}; \tag{3}$$

$$C = AB^T, \dot{A} = \dot{C}B, \dot{B} = \dot{C}^T A; \tag{4}$$

$$C = A^T B, \dot{A} = B\dot{C}^T, \dot{B} = A\dot{C},\tag{5}$$

where \dot{X} denotes the gradient of the parameter X. We present the algorithms for the three forms of multiplication with the optimal 3-D execution and communication efficiency as shown in the following pseudo-codes (Algorithm 1-6). Note that for each multiplication algorithm, other than the input matrices, we also need to specify the directions for them as well as the output matrix.

Algorithm 1 Forward $C = AB$	Algorithm 2 Backward $C = AB$		
Input: $A_{ijl}, B_{lji},$ directions y, x, z for A, B, C Output: C_{ilj} 1: All-gather A_{il} in y 2: All-gather B_{lj} in x 3: $C_{ilj} \leftarrow A_{il}B_{lj}$ 4: Reduce-scatter C_{ilj} in z 5: return C_{ilj}	Input: \dot{C}_{ilj} , A_{ijl} , B_{lji} directions y, x, z for A, B, C Output: \dot{A}_{ijl} , \dot{B}_{lji} 1: $\dot{A}_{ijl} \leftarrow \dot{C}_{ilj} B_{lji}^T$ in z, x, y 2: $\dot{B}_{lji} \leftarrow A_{ijl}^T \dot{C}_{ilj}$ in y, z, x 3: return \dot{A}_{ijl} , \dot{B}_{lji}		

Algorithm 3 Forward $C = AB^T$	Algorithm 4 Backward $C = AB^T$
Input: $A_{ijl}, B_{jli},$ directions y, x, z for A, B, C Output: C_{ilj} 1: All-gather A_{il} in y 2: All-gather B_{jl} in x 3: $C_{ilj} \leftarrow A_{il}B_{il}^T$	Input: $\dot{C}_{ilj}, A_{ijl}, B_{jli}$ directions y, x, z for A, B, C Output: $\dot{A}_{ijl}, \dot{B}_{jli}$ 1: $\dot{A}_{ijl} \leftarrow \dot{C}_{ilj}B_{jli}$ in z, x, y 2: $\dot{B}_{ijl} \leftarrow \dot{C}^T A_{ijl}$ in z, x, y
4: Reduce-scatter C_{ilj} in z	$2. D_{jli} \land C_{ilj} I_{ijl} \ \text{in } z, y, z$
5: return C_{ilj}	3: return A_{ijl}, B_{jli}

Algorithm 5 Forward $C = A^T B$	Algorithm 6 Backward $C = AB^T$
Input: $A_{ilj}, B_{ijl},$ directions y, x, z for A, B, C Output: C_{jli} 1: All-gather A_{ij} in y 2: All-gather B_{il} in x 3: $C_{jl} \leftarrow A_{ij}^T B_{il}$ 4: Reduce-scatter C_{jli} in z 5: return C_{jli}	Input: $\dot{C}_{jli}, A_{ilj}, B_{ijl}$ directions y, x, z for A, B, C Output: $\dot{A}_{ilj}, \dot{B}_{ijl}$ 1: $\dot{A}_{ilj} \leftarrow B_{jli} \dot{C}_{ilj}^T$ in x, z, y 2: $\dot{B}_{ijl} \leftarrow A_{ijl} \dot{C}_{ilj}$ in y, z, x 3: return $\dot{A}_{ilj}, \dot{B}_{ilj}$

Our 3-D parallel matrix multiplication can evenly distribute the computational cost to all the processors, where each processor only multiplies the submatrices of size (M/p, N/p) and (N/p, K/p). If we fix the problem size, the execution cost of our approach is supposed to be $(M/p)*(N/p)*(K/p) \approx$

 $O(1/p^3) = O(1/P)$. Furthermore, compared with 1-D and 2-D approaches, each communication operation in our 3-D approach moves data across a smaller number of processors. Each forward algorithm uses all-gather and reduce-scatter operations to move $(MN + NK + MK)/p^3$ across p processors in total. Therefore, the bandwidth cost of our approach is supposed to be $O(1/p^2) = O(P^{-2/3})$, while the latency cost is supposed to be $O(log(p)) = O(log(P^{1/3}))$.

3.1.3 Matrix-vector Operations

The logic to execute matrix-vector operations such C = A + b and C = A * b is similar. We present an example of the add operation as shown in Algorithm 7-8.

For the matrix-vector multiplication, the only changes from the above algorithms are to return $C_{ijl} = A_{ijl} * b_l$ for the forward pass, as well as to return $\dot{A}_{ijl} = \dot{C}_{ijl} * b_{ijl}$ and $\dot{b}_{ijl} = \sum_{ij} \dot{C}_{ijl} * A_{ijl}$ for the backward pass.

Algorithm 7 Forward $C = A + b$	Algorithm 8 Backward $C = A + b$		
Input: $A_{ijl}, b_{ijl},$ directions y, x, z for A, B, C	Input: \dot{C}_{ijl} , directions y, x, z for A, B, C		
Output: C _{ijl}	Output: $\dot{A}_{ijl}, \dot{b}_{ijl}$ 1: $\dot{A}_{ijl} \leftarrow \dot{C}_{ijl}$		
1: Broadcast b_{il} in y	2: $\dot{b}_{ijl} \leftarrow \sum_{ij} \dot{C}_{ijl}$ 3: if $i = l$ then		
2: All-gather b_l in x	4: Reduce-scatter \dot{b}_{ijl} in x 5: else		
3: $C_{ijl} \leftarrow A_{ijl} + b_l$	$\begin{array}{l} 6: \dot{b}_{ijl} \leftarrow \text{null} \\ 7: \text{ end if} \end{array}$		
4: return C _{ijl}	8: return $\dot{A}_{ijl}, \dot{b}_{ijl}$		

By taking advantage of balanced parameter storage, we can evenly distribute the computation cost of not only the matrix-vector operations but also the activations to all the processors. Their computation cost is supposed to be the same scale as the memory cost O(1/P).

3.2 Parallel Transformer layers



Figure 6: Outline of 3-D Parallel Transformer layers. Each m, n, k in [m, n, k] represents the size of the parameter stored on each processor. The arrows present the order of computation.

In this section, we describe the major implementation details of the Transformer model that uses our 3-D parallel operations.

To leverage 3-D model parallelism, we implement our new linear layer module and layer normalization module based on the 3-D parallel operations. The 3-D linear layer flattens an input X of size [b/p, s/p, h/p] into size $[b*s/p^2, h/p]$ first, and then uses Algorithm 1 and 7 to perform Y = XW + b with parameters W and b. Thus, after a 3-D linear layer, the input and output directions should

be exchanged. The 3-D layer normalization will not affect the directions, because it only applies matrix-vector adds and multiplications with the parameters γ and β .

We define b, s, n, h as the batch size, sequence length, number of attention heads and hidden size of the Transformer model on a p^3 processing cube. For ease of presentation, we do not discuss the embedding and output layers of the language model, as they usually depend on the downstream tasks. Then our implementation can basically divided into two modules: Self-Attention blocks and MLP blocks, as illustrated in Figure 6a and Figure 6b. Both the Self-Attention and MLP block include two 3-D linear layers, so that communication directions of their inputs and outputs are supposed to be the same. Thus, the input and output of each Transformer layer are also supposed to have the same communication direction.

Besides, in practice, it is therefore not necessary to track all the directions of 3-D parallel operations as shown in Algorithm 1-8, because we only need to exchange the input and output direction after the first linear layer of both Self-Attention and MLP blocks. For generalizability, we index the initial input, weight and output group as 0, 1, 2. We provide an input group index y for the first linear layer, so that the output group index is supposed to be z = 1 - y. After the layer, we take z as the new input group index, and return it to y = 1 - z after each Self-Attention or MLP block is completed.

4 **Experiments**

4.1 Setup

We evaluate our 3-D parallel Transformer model on TACC's Longhorn supercomputers [3]. Our testbed cluster consists of up to 16 GPU servers connected by Mellanox EDR Infiniband network. Each server has 2 20-core IBM Power 9 CPUs, 256GB memory and 4 NVIDIA V100 GPUs, so there are 64 GPUs in total. We store the training data, model checkpoints in a Hadoop Distributed File System (HDFS) via 1Gbps Ethernet.

We compare the performance of our approach against the existing state-of-the-art 1-D [17] and 2-D [21] model parallel approaches. For simplicity, we only evaluate the performance of the Transformer model itself, i.e. the consecutive Transformer layers, to highlight the efficiency of different parallelism. We evaluate the 1-D parallelism on 8,16,36 and 64 GPUs, the 2-D parallelism on a subset of 16,36 and 64 GPUs, as well as our 3-D approach on a subset of 8 and 64 GPUs.

4.2 Performance

4.2.1 Weak Scaling

We first evaluate the weak scaling performance, where we fix the network size on each processor, and scale up the number of processors. Table 1 presents the results of the weak scaling experiments, including the execution time for both forward and backward pass of the Transformer model. We also provide the average step time of each sequence, which is computed as

Average step time =
$$\frac{\text{forward time} + \text{backward time}}{\text{batch size}}$$
. (6)

We see that the 3-D parallelism has the slowest rising speed in the average step time, reaching the smallest value at the largest compute scale. The result implies that our approach is efficient to reduce the overhead of model parallelism, as it reaches the minimum communication cost.

4.2.2 Strong Scaling

Next, we evaluate the strong scaling performance of different model parallelism. This experiment aims to examine how much speedup each approach can achieve by using an increasing number of processors to execute the fix-sized problem.

The problem size and execution results are shown in Table 2. We see that our 3-D parallelism outperforms other approaches by achieving the smallest average step time on 64 GPUs, with 2.32X and 1.57X speedup over 1-D and 2-D approach, respectively.

1-D [17]	# GPUs 8 16	Batch size 60	Hidden size 2048	Forward time (s) 4.759	Backward time (s) 15.676	Average step time (s) 0.341
	36 64	40 30	6120 8192	13.515 13.915	31.822 32.890	1.133 1.560
2-D [21]	# GPUs 16 36 64	Batch size 192 288 384	Hidden size 4096 6120 8192	Forward time (s) 33.860 54.760 99.419	Backward time (s) 101.981 165.850 304.707	Average step time (s) 0.708 0.766 1.052
3-D	# GPUs 8 64	Batch size 192 384	Hidden size 2048 8192	Forward time (s) 30.096 79.349	Backward time (s) 81.212 125.037	Average step time (s) 0.580 0.672

Table 1: Comparison of weak scaling results. The number of processors increases from 8 to 64, while the number of parameters is fixed for each approach. For each of presentation, we mainly adjust the batch size and hidden size based on the number of processors, while fix the sequence length to 512. The bolded number represents the best result.

1-D [17]	# GPUs	Batch size	Hidden size	Forward time (s)	Backward time (s)	Average step time (s)
	8	12	3072	1.470	5.699	0.597
	16	12	3072	1.371	5.152	0.544
	36	12	3072	1.455	5.414	0.572
	64	12	3072	1.433	5.167	0.550
2-D [21]	# GPUs	Batch	Hidden	Forward	Backward	Average
		size	size	time (s)	time (s)	step time (s)
	16	24	3072	4.680	13.698	0.766
	36	24	3072	3.900	11.433	0.639
	64	24	3072	3.007	8.920	0.497
3-D	# GPUs	Batch	Hidden	Forward	Backward	Average
		size	size	time (s)	time (s)	step time (s)
	8	24	3072	3.249	9.120	0.515
	64	24	3072	2.494	6.129	0.359

Table 2: Comparison of strong scaling results. The problem size is fixed while the number of processors increases from 8 to 64. The bolded number represents the best result.

5 Conclusion

In this work, we introduce a 3-D intra-layer model parallelism algorithm for training huge neural models. We propose a load balanced design to store and execute linear layers with minimum memory and communication cost. By leveraging the 3-D model parallelism, we implement a 3-D parallel Transformer model and evaluate it on up to 64 GPUs. Compared with the existing 1-D and 2-D parallelism, our Transformer model achieves a significant speedup. However, it is still interesting to leverage our approach to train larger models on more processors. We expect to see promising advances of our work with larger-scale compute resources in the future.

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