Synergistic Tensor and Pipeline Parallelism

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Abstract

In the machine learning system, the hybrid model parallelism combining tensor parallelism (TP) and pipeline parallelism (PP) has become the dominant solution for distributed training of Large Language Models (LLMs) and Multimodal LLMs (MLLMs). However, TP introduces significant collective communication overheads, while PP suffers from synchronization inefficiencies such as pipeline bubbles. Existing works primarily address these challenges from isolated perspectives, focusing either on overlapping TP communication or on flexible PP scheduling to mitigate pipeline bubbles. In this paper, we propose a new synergistic tensor and pipeline parallelism schedule that simultaneously reduces both types of bubbles. Our proposed schedule decouples the forward and backward passes in PP into fine-grained computation units, which are then braided to form a composite computation sequence. This compositional structure enables near-complete elimination of TP-related bubbles. Building upon this structure, we further design the PP schedule to minimize PP bubbles. Experimental results demonstrate that our approach improves training throughput by up to 12% for LLMs and 16% for MLLMs compared to existing scheduling methods. Our source code is avaiable at https://github.com/MICLAB-BUPT/STP.

1 Introduction

Distributed systems [6, 23, 38, 11, 31] have become the cornerstone for the training of large-scale machine learning models [1, 35, 28, 4, 19, 26, 27, 20], particularly since model scales have grown to tens of billions of parameters. Data parallelism [12, 15, 5] is commonly employed to accelerate training and is most effective for relatively smaller models. As the scale of the model increases, researchers have turned to model parallelism [10, 32, 21], which partitions the model into smaller components and distributes them between multiple devices. Model parallelism primarily consists of two strategies: tensor parallelism (TP) [33] and pipeline parallelism (PP) [7, 23, 30]. Tensor parallelism partitions model weights across devices according to predefined rules, thereby reducing per-device memory requirements. While TP alleviates GPU memory pressure to some extent, it introduces additional collective communication operations within TP groups, referred to as TP bubbles that exhibit significant growth with increasing TP size, as shown in Figure 1. For instance, the TP bubbles account for 27.5% of the overall time in the configuration of TP=8 and sequence length of 6,144, which can significantly degrade the performance. In contrast, pipeline parallelism divides the model into chunks along the layer dimension, which are assigned to PP stages according to the PP strategy. Activations and gradients are then transmitted among PP stages during the forward and backward passes. This strategy enables efficient utilization of computational resources but requires careful synchronization between stages to minimize idle time, commonly referred to as PP bubbles.

To mitigate TP bubble issues, existing studies [37, 8, 2, 25] aim to overlap communication with computation at the kernel level, such as customized CUDA kernels [2], or at the hardware level,

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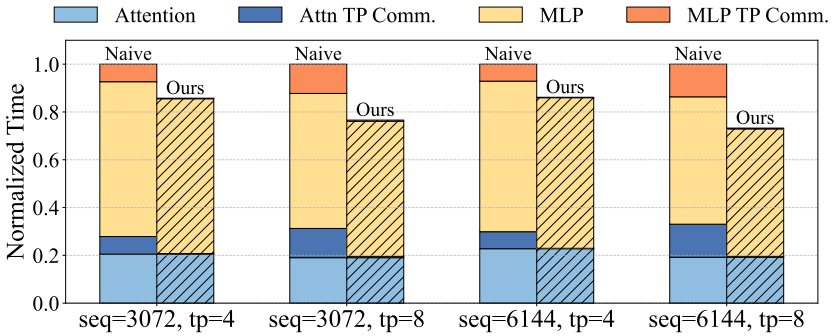


Figure 1: Speedup of overlapping TP communication with computation in PP within a Transformer layer of Qwen2 [39] in forward pass. The proportion of TP communications grows significantly with the increased TP size, which are effectively overlapped in our schedule compared with the naive implementation.

where specialized hardware mechanisms like the track-and-trigger system [25] are employed. By carefully scheduling paired decomposed communication and computation chunks, these methods effectively reduce overall execution time. As for PP bubbles, GPipe [7] reduces pipeline bubbles by splitting the global batch into microbatches. Subsequently, 1F1B [22] improves upon GPipe by scheduling backward passes earlier, thereby optimizing peak memory footprint. Furthermore, 1F1B-I [23] reduces the bubble rate by introducing virtual stages assigned to individual devices. More recently, Zero Bubble [30] decouples the full backward pass into separate activation and weight gradient computations, enabling more flexible scheduling and achieving a significantly lower PP bubble rate.

In practice, hybrid model parallelism, particularly the combination of PP and TP, has become the dominant approach for large-scale model training. However, most of the aforementioned works primarily focus on optimization from isolated perspectives, generally yielding limited enhancements. Inspired by studies [17, 14] that integrate two kinds of parallelism strategies for better optimization, our work aims to integrate PP and TP from a synergistic perspective. Specifically, our method leverages the abundant computation operations inherent in PP to overlap the TP bubbles and employs precise scheduling to mitigate the PP bubbles. Firstly, we decouple the forward and backward passes of the model chunk within each stage of PP into fine-grained computation units. By interleaving forward and backward computation units to construct execution blocks, we achieve near-zero TP idle time as shown in Figure 1, where TP communication and the fine-grained computation units in PP execute in parallel. Building upon these blocks, we further design a PP schedule with a low bubble rate and balanced memory footprints across stages. Additionally, we provide an enhanced variant of our schedule that incorporates activation offloading, serving as a preliminary attempt under limited memory conditions. Our main contributions are summarized as follows:

- We rethink hybrid model parallelism from a synergistic perspective and decouple the forward and backward passes of PP into fine-grained computation units, which are interleaved together to form braided execution blocks that effectively eliminate TP communication bubbles at the scheduling level.
- We design a novel PP schedule that synergistically integrates with TP based on the braided execution blocks. This schedule features a "V"-shape dataflow that achieves balanced memory footprints and a significantly reduced PP bubble rate.
- We conduct extensive experiments on popular LLMs and MLLMs of various scales to validate the universality and effectiveness of our method. The results demonstrate that our proposed schedule improves throughput by up to 16% compared to the existing methods.

2 Related Work

Tensor Parallelism. Tensor parallelism [33, 23, 14, 37, 8, 2] partitions tensors across devices to reduce per-device memory usage but introduces communication overhead due to synchronization requirements. This problem becomes more pronounced with TP sizes increase, where the limited

inter-device bandwidth (*e.g.*, systems without NVLink [24]) can severely degrade training efficiency. Several prior works [37, 8, 2] optimize this kind of collective communication by breaking down both communication and corresponding computation operations into sequences of smaller chunks. Subsequently, they carefully coordinate the execution of these granular units to achieve acceleration, often through the intricate fusion of computation and communication kernels, along with complex hardware control. In contrast, our proposed schedule optimizes TP communication at the scheduling or software level, providing a more accessible and user-friendly approach.

Pipeline Parallelism. Pipeline parallelism [16, 11, 34, 9, 18, 13, 17] divides the entire model into smaller chunks using a variety of strategies. GPipe [7] reduces PP bubbles by splitting the global batch into smaller micro-batches. Building on this, PipeDream [22] improves upon GPipe by advancing the backward computation to further reduce memory usage. 1F1B-I [23] and Hanayo [18] further introduce additional virtual stages to lower the bubble rate. More recently, Zero Bubble [30] decouples the backward computation into activation gradient and weight gradient computation to achieve a near-zero PP bubble schedule. However, these existing schedules tend to address PP bubbles in isolation. In this paper, we design an integrated approach that concurrently minimizes both TP and PP bubbles by synergistically combining these two parallelism techniques.

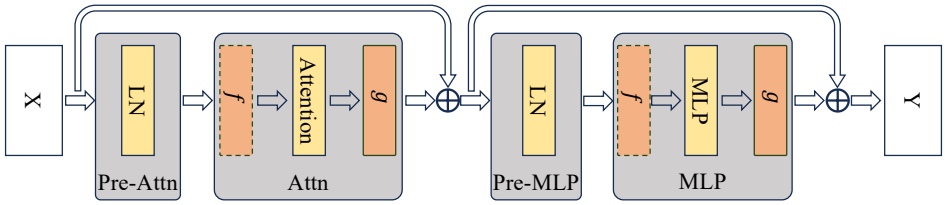
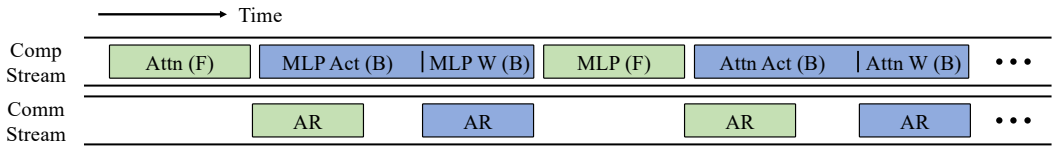
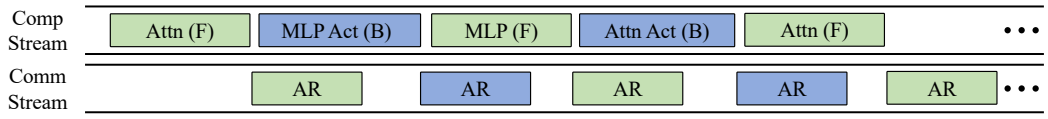


Figure 2: Illustration of the main computation and communication operation in a single TP Transformer layer. f is an identity operation in forward while All-Reduce in backward. g is opposite to f.



(a) Execution block with forward and full backward.



(b) Execution block with forward and activation backward.

Figure 3: Two types of execution blocks that braid the forward (F) and backward (B) computation units to overlap the TP communications (All-Reduce), denoted as AR.

3 Braided Execution Block

Although TP reduces memory consumption, it introduces additional communication overhead after the Attention and MLP computations in both the forward and backward passes, as illustrated in the orange blocks in Figure 2. As shown in the blue blocks of Figure 3a, the communication represented by the blocks in the communication stream can be naturally overlapped with the weight gradient computation during the backward pass, where TP communication (All-Reduce) and weight gradient computation run in parallel. However, the communication in the solid blocks during the forward pass cannot be easily overlapped with other operations at the software level due to data dependencies, leading to massive TP bubbles. To address this TP bubble issue, we design two types of execution blocks that overlap TP communication with PP computation through braiding forward and backward computation units, as shown in Figure 3. These blocks serve as the foundation of our schedule.

Specifically, we decompose the entire Transformer layer into several fine-grained computation units: the Pre-Attn unit, Attn unit, Pre-MLP unit, and MLP unit. The units from the forward and backward passes are then interleaved sequentially to form a braided execution block, as shown in Figure 3a. Moreover, both the Attn and MLP units in backward passes are further split into two components: activation gradient computation and weight gradient computation, following Zero Bubble [30]. When necessary, we activate the separation of weight gradient computations to balance the workload and reduce pipeline bubbles. This separation does not disrupt the execution blocks, as the subsequent forward computation can fill the bubbles introduced by the separation, as shown in Figure 3b. The Pre-Attn and Pre-MLP units are inserted into the computation stream according to their computational dependencies. All these operations only involve model-level modifications, making our approach more user-friendly compared to kernel-level implementations.

Furthermore, considering the residual computations after the Attn and MLP units that introduce additional data dependencies and increase engineering complexity for backward passes, we modify the forward and backward computations to fuse the residual computation into the Attn and MLP units before applying operation g. This modification preserves computational equivalence and does not affect model convergence. The modified forward computation of the Attn unit for a single TP rank can be formulated as follows:

$$X_{ln} = LayerNorm(X), \quad X_{attn} = AR(Attention(X_{ln}) + \frac{detach(X)}{t}), \tag{1}$$

where t denotes the tensor parallel size, $detach(\cdot)$ is an operation that stops gradient computation of X, $Attention(\cdot)$ is the attention computation performed without any communication, and $AR(\cdot)$ represents the All-Reduce communication operation. The gradient computation $g(X)$ of the hidden state X is then formulated as the following:

$$g(X) = AR\left(\frac{\partial X_{attn}}{\partial X_{ln}}\right) \cdot \frac{\partial X_{ln}}{\partial X} + 1, \tag{2}$$

where the term $+1$ accounts for the gradient contribution from the residual connection. Similarly, the MLP unit adopts a comparable computation fusion strategy.

4 Pipeline Parallelism Schedule

We begin by introducing several key principles that facilitate the construction of the overall schedule in Section 4.1 and then introduce the proposed schedule in Section 4.2. Following this, we present a theoretical analysis of the PP and TP bubbles and peak memory in Section 4.3. Finally, we propose an enhanced variant of our schedule to accommodate scenarios with limited memory in Section 4.4.

4.1 Building Principles

To ensure an effective pipeline schedule, we outline several guiding principles aimed at optimizing memory efficiency and minimizing bubbles.

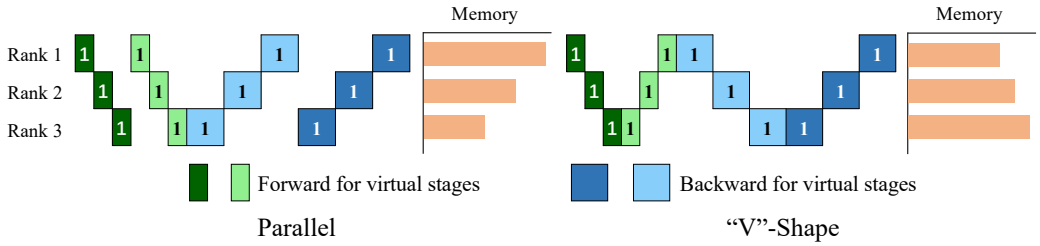


Figure 4: Comparison between parallel and "V"-shape pipeline flow for microbatch 1, which shows improved memory balance across stages. That is attributed to the early backward pass on device 0.

Balanced Memory Footprint: As discussed in [29, 18], the 1F1B-I [23] often leads to a memory bottleneck on the first device due to the parallel dataflow of virtual stages, while subsequent stages often have underutilized memory resources. This imbalance results in inefficient resource usage. To

tackle this issue, current scheduling methods [18, 29, 17] utilize a “V”-shape scheduling strategy to achieve a more balanced distribution of peak memory across all devices (see Figure 4). We follow this principle by implementing a "V"-shape dataflow for our virtual stages to optimize memory efficiency, which also supports the scheduling of braided execution blocks for improved overall performance.

Bubble Minimization: The braided computation-communication execution blocks, as detailed in Section 3, illustrate the arrangement of computation units. The practical construction of these blocks follows two primary patterns: (1) pairing the forward units of one virtual stage with the backward units of another, or (2) braiding the forward and backward units of the same model chunk across different microbatches. The selection of the building pattern is closely tied to the characteristics of virtual stages in PP. Specifically, when partitioning models into virtual stages, it is essential to maintain approximately equal execution times across these stages to mitigate pipeline bubbles. For MLLMs, a significant disparity often exists between the vision encoder (*e.g.*, ViT) and the Language Model (LM) due to differences in their hidden sizes. This presents a key challenge for multimodal models, where earlier virtual stages typically contain more ViT layers, while later stages consist of fewer LM layers to achieve balanced execution times. However, the imbalance in the number of computation units across virtual stages limits the effectiveness of pattern (1), as mismatched unit counts prevent efficient hiding of TP communication during cross-virtual-stage pairings. In contrast, pattern (2), which involves overlapping the forward and backward units of the same chunk, more effectively minimizes the TP bubbles. Therefore, we adopt pattern (2) to construct the basic blocks for universality, especially considering the multimodal models.

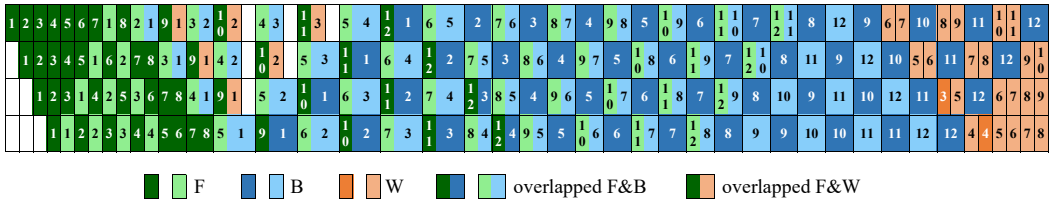


Figure 5: Synergistic tensor and pipeline parallel schedule with the setting of 4 devices and 12 microbatches. The dark and light pieces indicate the computation of model chunks 0 and 1, respectively. F, B, and W represent the forward, backward, and backward for weight gradients, respectively.

4.2 Synergistic Tensor and Pipeline Parallel Schedule

Based on the above building principles, we construct a synergistic tensor and pipeline schedule, which implements a “V”-shape dataflow across stages for a single microbatch, as illustrated in Figure 5. Similar to existing schedules [22, 23, 30], our proposed method comprises three main phases: the warm-up phase, the steady phase, and the cool-down phase. First, the warm-up phase begins with the maximum feasible number of in-flight microbatches before the commencement of the first backward pass. This helps to maintain a low PP rate and facilitates the construction of the braided blocks, as the backward passes of earlier microbatches form the blocks in conjunction with the forward passes of subsequent microbatches. The number of microbatches involved in the warm-up phase is determined by the number of stages. During this phase, the overlapped forward and backward (F&B) start from the braided computation of the first and second microbatches, and weight gradient separation is activated to quickly propagate gradients to the next stage, except for the last stage.

After several iterations of overlapped forward and weight (F&W) and F&B, the schedule transitions into the steady phase. In this phase, weight separation is deactivated as long as new microbatches continue to arrive. Under these conditions, the system performs one F&B for model chunk 1, followed by one F&B for chunk 0. When the supply of microbatches is exhausted, maintaining full F&B becomes infeasible, and the process degrades into a full backward pass followed by a separated F&B. During this degraded phase, weight separation is reactivated to align the time of F&B with that of the full backward pass. During the cool-down phase, the backward passes for all remaining in-flight microbatches are completed. The pipeline bubbles are filled with stored weight gradient computations from earlier steps. Moreover, activating weight separation during the steady phase leads to memory accumulation, as the corresponding weight computations remain pending until the final steps. Therefore, the saved activations required for the weight gradients are offloaded to the CPU in parallel with the computation streams and reloaded when necessary.

4.3 Theoretical Analysis

We define the number of PP stages and microbatches as p and m respectively, where $p \ll m$. For simplicity, multimodal models are not taken into account in this context. For LLMs, we assume the model is evenly divided into chunks along with the layer dimension, and each microbatch requires the same activation memory M_a for each model chunk across all devices. The computation time for the forward pass of one chunk is denoted as T_F, while the durations of activation and weight gradient computation are T_B and T_W, respectively. The TP communication time of one model chunk is represented as T_{AR}, which remains consistent for both forward and backward passes.

Table 1: Comparison between 1F1B-I, Zero Bubble V, and our proposed schedule on theoretical PP bubble size, non-overlapped TP communication bubble, and peak activation memory.

Schedule	PP Bubble	TP Bubble	Peak Act. Memory
1F1B-I	$(p-1)*(T_F+T_{AR}+T_B+T_W)$	$2*m*T_{AR}$	$(3*p-2)*M_a$
ZB-V	$(p-1)*(T_F+2T_{AR}+T_B-2T_W)$	$4*m*T_{AR}$	$2*p*M_a$
Ours	$(p-1)*(T_F+T_{AR}+T_B-T_W)$	$(2*p+1)*T_{AR}$	$3*p*M_a$

As shown in Table 1, 1F1B-I [23] with 2 virtual stages requires $(3*p-2)*M_a$ peak activation memory for the first device, which progressively decreases as the stage index increases. In the backward pass, the TP communications are overlapped naturally, but the TP communications in the forward pass are non-overlapped, resulting in a total TP communication time is $2*m*T_{AR}$. In contrast, Zero Bubble V (ZB-V) [29] achieves a smaller theoretical bubble size of $(p-1)*(T_F+2T_{AR}+T_B-2T_W)$ and maintains the lower peak activation memory than that of 1F1B-I. However, due to the decoupling of the backward into activation and weight gradient computations, the TP communication in both forward and activation backward pass becomes non-overlapped, leading to a total TP communication time of $4*m*T_{AR}$ and a larger practical bubble size. Our schedule exhibits the approximate bubble size of $(p-1)*(T_F+T_{AR}+T_B-T_W)$ compared to the ZB-V schedule, which is much smaller than that of 1F1B-I. And it achieves substantially reduced TP overheads, benefiting from the overlapped computation and communication, albeit with a trade-off in the peak activation memory.

4.4 Enhanced Pipeline Schedule

Considering the practical demands of limited CUDA memory, we attempt to reduce the peak memory footprint of our scheduling strategy. The elevated peak memory usage primarily stems from two phases: the warm-up phase, where the number of in-flight microbatches is maximized to maintain a low bubble rate, and the steady phase, where activations from model chunk 0 persist for an extended period before being released, denoted as lifespan. Existing methods [40, 34] such as activation checkpoint and offloading have been used to reduce memory. However, checkpointing introduces an extra forward pass during backward, increasing execution time. Thus, activation offloading offers a better trade-off between memory reduction and e2e performance, when high-speed bandwidth is available between the host and the device.

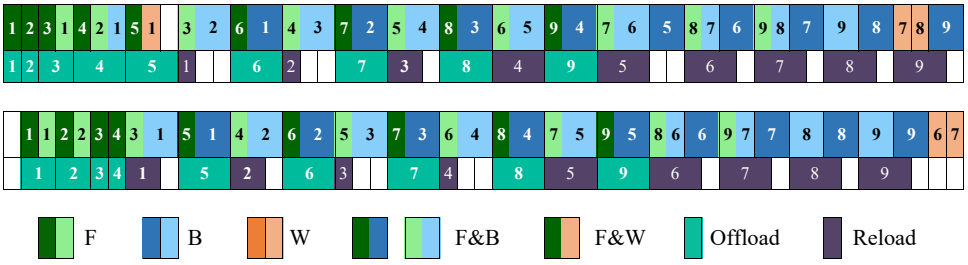


Figure 6: Illustration of our proposed schedule with offloading and reloading for one microbatch in warm-up and steady phase with the setting of PP size 2.

During the warm-up phase in Figure 6, where memory usage accumulates rapidly, the activations of chunk 1 have a short lifespan and are thus deprioritized for offload. The offload time T_o, determined

by the offloading ratio α, is restricted to be less than the forward time T_F to avoid interference with subsequent operations. In the steady phase, chunk 0 activations persist much longer than those in chunk 1, making them the primary target for offloading. The offload ratio α in this phase can be set higher than in the warm-up phase due to the braided execution blocks. To minimize PCIe bandwidth contention caused by frequent dual CPU-GPU data transfers, we avoid offloading chunk 1 activations, ensuring they can be reloaded in time without disrupting computation. The ratio α is adjusted based on hardware characteristics such as PCIe bandwidth and FLOPs.

5 Experiments

5.1 Setup

We evaluated our proposed schedule on the series of Qwen2 (LLM) [39] and Qwen2-VL (MLLM) [36] models, as detailed in Table 2. Meanwhile, Flash Attention 2 [3] is leveraged in all models for efficiency. Our implementation is built upon the open-source Megatron-Core project [33] and tested on up to 32 NVIDIA A800 SXM4 80G GPUs distributed across 4 nodes. Each experimental result is recorded after several warm-up iterations to ensure stability.

In LLM scenarios, we adopt the approach described in [30], uniformly splitting the model while ensuring that the last stage contains two fewer layers than the other stages, considering the large vocabulary size of 152,064 in Qwen. In MLLM scenarios, the ViT encoder is assigned to the first virtual stage on device 0, and the LM model is uniformly distributed across the remaining virtual stages, and the last virtual stage also contains two fewer layers compared to the other stages.

To be specific, our experiments primarily concentrate on the following pipeline parallel schedules: a) interleaved 1F1B (1F1B-I), as implemented in Megatron-LM [23], which reduces the bubble ratio by interleaving stages among workers but slightly increases memory footprint; b) ZB-V, introduced in [29], which achieves a balanced peak memory distribution through a "V"-shape dataflow; and c) our proposed schedule. For consistency, all schedules are configured with two virtual stages per device, and the implementations are based on open-source codebases.

Table 2: Model configurations evaluated on the experiments.

Model	Scale	ViT Layers	ViT Heads	ViT Dim.	LM Layers	LM Q Heads	LM KV Heads	LM Dim.
LLM	12.1B	-	-	-	30	40	8	5120
LLM	26.3B	-	-	-	46	56	8	7168
MLLM	14.9B	32	16	2048	33	40	8	5120
MLLM	28.8B+	26	16	4096	40/43	56	8	7168

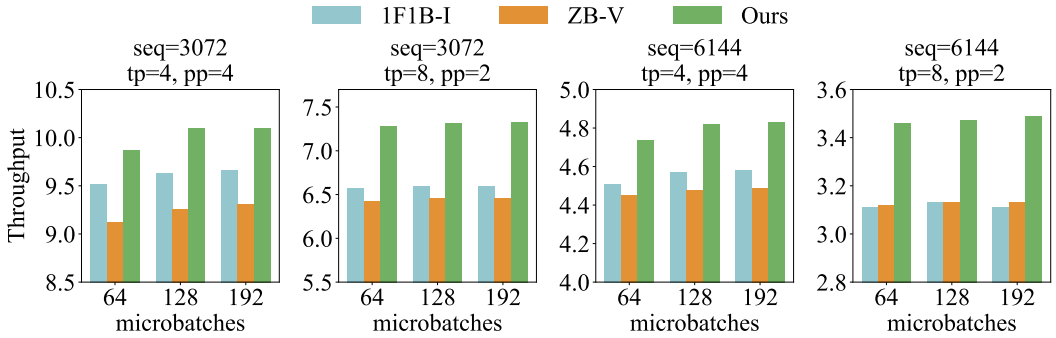


Figure 7: Experiment results on 12.1B LLM across 16 GPUs in terms of throughput (samples per second).

5.2 Comparison with Existing Schedules on LLM

In Figures 7 and 8, we report experimental results by evaluating Qwen2 on 2-node and 4-node setups, respectively, showing the achieved throughput under various pipeline strategies, sequence lengths,

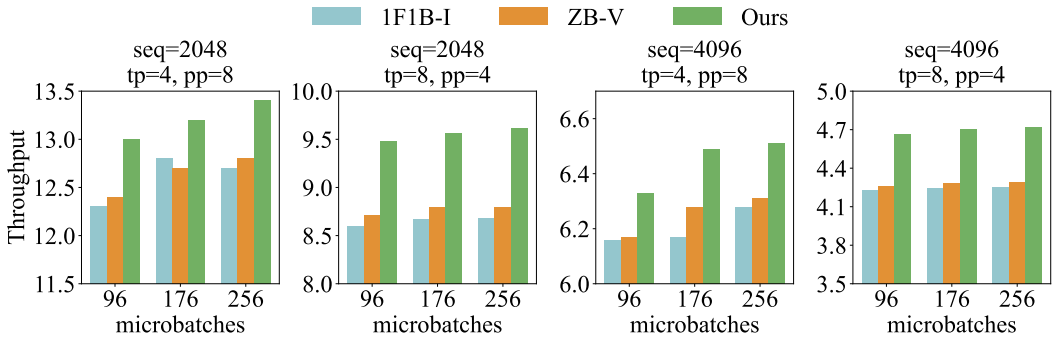


Figure 8: Experiment results on 26.3B LLM across 32 GPUs in terms of throughput.

and model scale configurations. Our proposed schedule outperforms all other strategies across all settings in terms of throughput. As shown in the right part of Figure 7, our method achieves a maximum improvement of 12.2% over 1F1B-I. This performance gain is attributed to the large TP size of 8, the long sequence length of 6,144, and the low PP size of 2 used in the experiments. As illustrated in Figure 1, TP-related bubbles occupy a significant proportion under TP size 8, especially for attention units, which are effectively mitigated by our scheduling approach.

However, the performance improvements under PP=8 in Figure 8 are less pronounced. This is due to the explicit pipeline communication in our schedule, which is executed immediately after computation and cannot be overlapped with computation, thereby negatively impacting performance. Nevertheless, our scheduling strategy still outperforms the other two methods. The highest throughput improvements for both 12B and 26B LLMs are achieved at TP=8, demonstrating that our method offers substantial potential when scaling to larger models with TP=8, even TP=16. Notably, ZB-V demonstrates comparable or even worse performance than 1F1B-I. Since ZB-V is based on the decoupling of the full backward pass, which exposes previously overlapped TP bubbles during the full backward in 1F1B-I and introduces additional bubble overheads, thereby eliminating the potential benefit of reduced PP bubbles from decoupling.

Furthermore, we show the peak activation memory footprints with 4 and 2 PP stages in Figure 9. While our schedule exhibits a slightly higher peak memory footprint, it can achieve optimal throughput, especially under memory-unconstrained scenarios. For memory-limited scenarios, we introduce an enhanced variant that significantly reduces memory footprints while maintaining comparable throughput, detailed in Section 5.4.

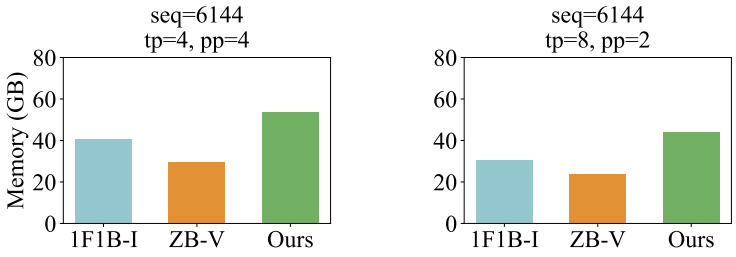


Figure 9: Peak activation memory footprint tested on 12.1B LLM across 2 nodes.

5.3 Comparison with Existing Schedules on MLLM

As shown in Tables 3, we present experimental evaluations of Qwen2-VL on 2-node and 4-node setups, respectively, which report throughput and peak activation memory under various configurations, including ViT lengths, LM lengths, and model scale parameters. For the PP=4, we carefully adjust the ViT and LM sequence lengths to balance computational workload across virtual stages by ensuring the FLOPs of the ViT approximately match those of individual virtual stages. In contrast, for PP=2 and PP=8, we intentionally maintain disparities in ViT/LM FLOPs to conduct diverse workload scenarios. Our scheduling approach demonstrates superior performance compared to baseline methods in all balanced computational scenarios. Notably, we observe a maximum throughput improvement

Table 3: Experimental results for the 14.9B, 28.8B, and 30.3B MLLMs, showing throughput (samples per second) and peak activation memory footprint (GB). mbs denotes the number of microbatches.

Model	ViT Length	LM Length	TP	PP	Schedule	mbs 64	mbs 128	mbs 192	Memory
1.7B ViT	3136	5120	4	4	1F1B-I	4.36	4.44	4.46	40
					ZB-V	4.25	4.30	4.31	**30**
13.2B LM					Ours	**4.53**	**4.63**	**4.65**	56
			8	2	1F1B-I	2.42	2.44	2.46	**26**
16 GPUs					ZB-V	2.48	2.49	2.49	30
					Ours	**2.86**	**2.86**	**2.87**	51

Model	ViT Length	LM Length	TP	PP	Schedule	mbs 96	mbs 176	mbs 256	Memory
5.6B ViT	1600	3072	4	8	1F1B-I	5.79	5.89	5.85	60
					ZB-V	5.90	5.97	6.01	**48**
23.2B / 24.7B LM					Ours	**5.97**	**6.19**	**6.19**	69
	2304	5120	8	4	1F1B-I	3.37	3.40	3.40	43
32 GPUs					ZB-V	3.51	3.53	3.53	**38**
					Ours	**3.72**	**3.80**	**3.80**	47

of 11.7% in the configuration with TP=8 and PP=4, which is significantly higher than the 2% improvement in TP=4 and PP=4, compared to 1F1B-I. This trend aligns with observations from LM experiments, indicating that larger TP sizes generally yield greater performance gains.

A particularly notable result is the 16.7% performance improvement achieved by our schedule in the PP=2 setting, where the ViT component has relatively lower computational intensity compared to other model chunks. In this case, the lowest peak memory footprint is achieved by 1F1B-I in stage 1, where only a few microbatches are in-flight and the memory in ViT is much smaller compared to that in LM. In the PP=8 scenario, where the ViT's FLOPs exceed those of the LM chunks, our schedule and ZB-V achieve comparable throughputs at $mbs = 96$. However, as the number of microbatches increases, our approach demonstrates superior scalability and robustness, gaining more improvements compared to ZB-V and 1F1B-I.

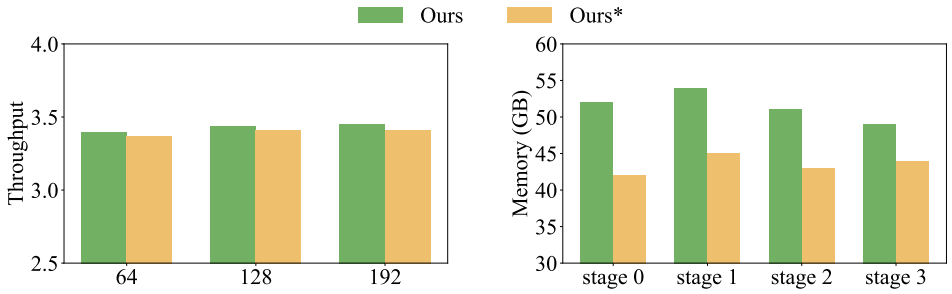


Figure 10: Experimental results in terms of throughput and peak activation memory footprints over 4 PP stages on the 12.1B LLM. $*$ indicates the enhanced variant with offloading.

5.4 Efficiency of Our Enhanced Schedule

Due to the limited PCIe bandwidth of the A800, where the effectiveness of the offloading variant cannot be fully demonstrated, we perform experiments on 16 NVIDIA H20 GPUs, which are equipped with PCIe Gen 5 interconnection. As shown in Figure 10, the offloading variant incurs a negligible throughput degradation due to additional CPU overheads associated with data transmission. However, as demonstrated in the right part of Figure 10, the memory footprints across all stages are approximately equal, indicating our schedule effectively utilizes the memory resources to improve

the throughput. And the offloading strategy achieves a peak memory reduction ranging from 10% to 19.2%, with the resulting peak memory footprint being close to that of 1F1B-I (40G).

5.5 Results under Maximized Resource Utilization

We conduct experiments on 16 NVIDIA H20 96GB GPUs, adjusting the microbatch size across various parallel configurations to maximize memory utilization and achieve optimal throughput and Model FLOPs Utilization (MFU). As shown in Table 4, our proposed method delivers superior performance under maximized memory utilization. Specifically, under the TP=2, PP=8 configuration, our enhanced schedule achieves slightly higher throughput (2.74 samples/s) and MFU (92.86%) compared to 1F1B-I, despite the lower proportion of TP bubbles on H20 GPUs (see the Appendix D for details), while maintaining a lower and more balanced memory footprint of 68 GB.

Table 4: Experiment results on 12.1B LLM under maximized memory utilization, which are evaluated on 16 H20 GPUs. $*$ denotes the enhanced variant of our schedule with activation offloading.

Configurations	Parallelism	mbs	Schedules	Throughput	MFU	Memory
mbs=192 seq_len=8192	TP=2 pp=8	1	1F1B-I	2.72	92.09	76
			ZB-V	2.61	88.36	54
			Ours	OOM		
			Ours*	**2.74**	**92.86**	68
	TP=4 pp=4	1	1F1B-I	2.47	83.62	53
			ZB-V	2.41	81.59	38
			Ours	2.52	85.32	71
		2	1F1B-I	OOM		
			ZB-V	2.47	83.62	75
			Ours*	OOM		
	TP=8 pp=2	1	1F1B-I	2.06	69.74	40
			ZB-V	2.07	70.08	31
			Ours	2.12	71.78	57
		2	1F1B-I	2.14	72.45	76
			ZB-V	2.18	73.81	61
			Ours*	OOM		
		3	1F1B-I	OOM		
			ZB-V	1.74	58.91	90
			Ours*	OOM		

6 Conclusion

In this paper, we presented a novel hybrid parallel strategy that synergistically integrates tensor and pipeline parallelism for distributed training of LLMs and MLLMs. By decomposing Transformer layers into fine-grained computation units and interleaving forward and backward computations within each PP stage, we constructed execution blocks that effectively overlap TP communication bubbles. Based on these blocks, we designed a "V"-shape PP schedule, which achieves balanced memory across stages and significantly reduces both TP and PP bubbles, albeit at the cost of increased peak memory. Experimental results demonstrated that our approach consistently outperforms existing scheduling methods on both LLMs and MLLMs. We also presented an enhanced variant incorporating offloading to better accommodate memory-constrained scenarios. In future work, we plan to explore more memory- and throughput-efficient hybrid schedules in the large-scale machine learning system.

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Question: For crowdsourcing experiments and research with human subjects, does the paper include the full text of instructions given to participants and screenshots, if applicable, as well as details about compensation (if any)?

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Question: Does the paper describe the usage of LLMs if it is an important, original, or non-standard component of the core methods in this research? Note that if the LLM is used only for writing, editing, or formatting purposes and does not impact the core methodology, scientific rigorousness, or originality of the research, declaration is not required.

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- Please refer to our LLM policy (`https://neurips.cc/Conferences/2025/LLM`) for what should or should not be described.

Appendix

A The Warm-Up Phase of the Pipeline Schedule

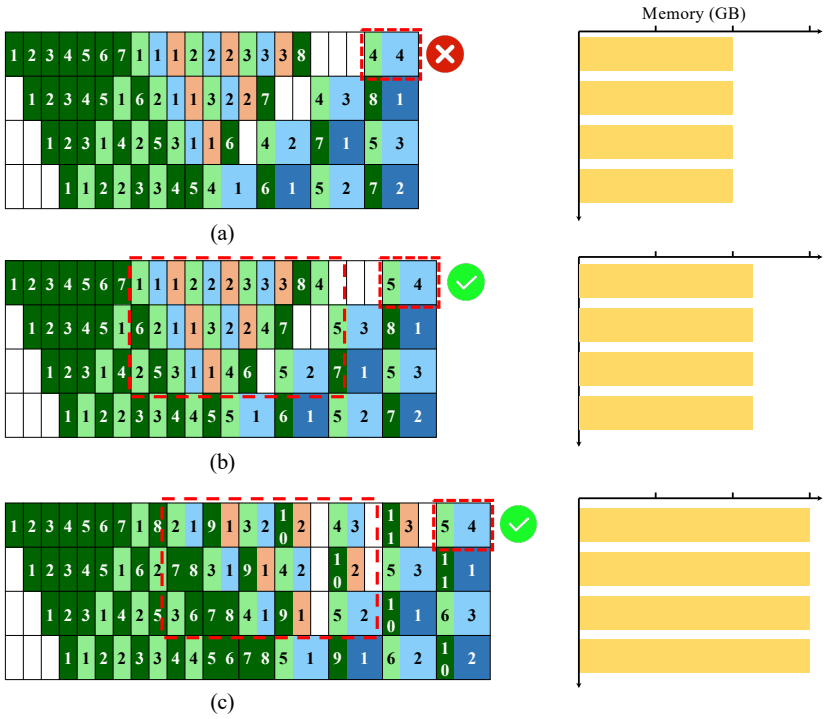

Figure 11: The construction of the warm-up phase: (a) wrong warm-up phase; (b) memory-efficient warm-up phase; (c) throughput-efficient warm-up phase.

The guiding principle for constructing the warm-up phase is to ensure the correct execution of overlapped forward and backward passes. As illustrated at the top of Figure 11, a key requirement is that overlapping between forward and backward passes must occur across different microbatches. Specifically, the microbatch index in the forward pass should be greater than that in the backward pass. To satisfy this condition, an additional forward pass is required before the overlapped F&B execution begins, as shown in Figure 11(b). However, this approach necessitates decoupling the backward pass into activation and weight gradient computations, which exposes TP communication and introduces additional PP communication overheads. Please refer to Section B for more details about the memory-efficient warm-up phase.

B Comparison with Other Schedules

We compare 1F1B-I [23], ZB-V [29], and our proposed schedule under identical configurations: 4 pipeline stages, 2 virtual stages per pipeline stage, and 12 microbatches, as illustrated in Figure 12. Intuitively, both ZB-V and our schedule have a similar number of PP bubbles, which are significantly fewer than those in 1F1B-I. The PP bubbles in 1F1B-I primarily result from the warm-up and cool-down phases. In the warm-up phase, the parallel dataflow across virtual stages results in a large number of bubbles. For instance, the long lifespan of virtual stage 2 for microbatch 1 cannot be efficiently filled without introducing additional forward passes from more microbatches, which would increases the peak memory of the stage 1. Consequently, 1F1B-I incurs greater PP bubble overheads during the warm-up phase. Meanwhile, the bubbles in the cool-down phase are inevitable due to inherent data dependencies.

Compared to ZB-V, our schedule results in a small number of PP bubbles at the end of the warm-up phase, which are attributed to the relatively long execution time and specific PP dataflow pattern

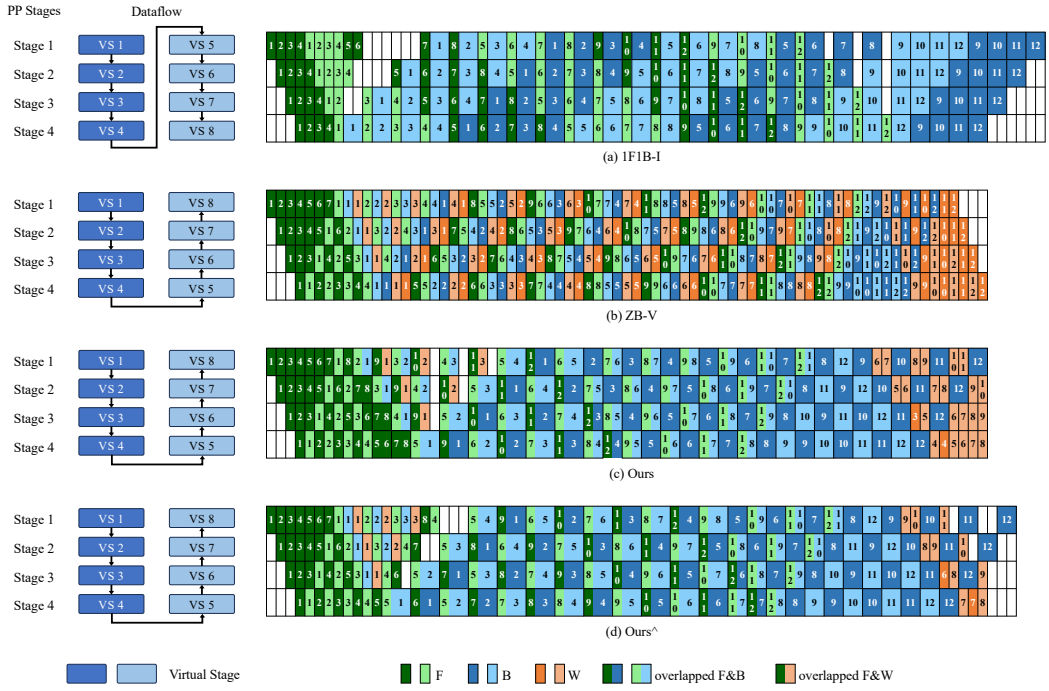

Figure 12: Synchronous pipeline parallelism schedules compared in our work, with 4 pipeline stages and 12 microbatches within a training iteration. Dark colors denote the first virtual stage and light colors are the second virtual stage. ˆdenotes the tensor and pipeline schedule beginning with the memory-efficient warm-up phase.

of the overlapped F&B blocks. In general, the activation gradient computation time T_B satisfies $T_B > T_W$, where T_W is the weight gradient computation time. As a result, small bubbles also appear at the end of the cool-down phase, and their magnitudes are approximately equal for both ZB-V and our proposed schedule.

Moreover, we also present schedule Oursˆ (d), which begins with a memory-efficient warm-up phase, as illustrated in Figure 12. Although schedule (d) has a lower peak memory footprint compared to our standard schedule (c), it introduces additional PP bubbles towards the end, negatively impacting throughput performance. Therefore, for scenarios involving large-scale model training with large TP sizes and ample memory availability, we prefer schedule (c) for its higher performance. Our enhanced schedule variant, which includes activation offloading, is preferable for reducing peak memory usage, assuming sufficient bandwidth. Schedule (d) is suitable only for scenarios with extremely limited memory and large TP overheads.

C Detailed Experimental Results on LLMs

We present detailed experimental results based on the 12.1B and 26.3B Qwen2 models, as summarized in Tables 5, 6, and 7. Notably, the GPU memory footprint reported in Table 5 is slightly higher than the theoretical estimate. We attribute this discrepancy primarily to practical aspects of our engineering implementation, such as the implementation of the fine-grained computation units and the decoupling of weight gradient computation. For example, under TP=8, profiling the activation memory of one microbatch per virtual stage shows that ZB-V consumes 3.6 GB, while our approach uses 4.3 GB, an increase of nearly 20%. Although this issue has no impact on throughput, we plan to further refine the engineering implementation to reduce this overhead in future work.

Table 5: Experimental results on 12.1B and 26.3B LLMs in terms of peak memory (GB), where the microbatch sizes of samples with sequence length 3072 and 2048 are set to 2.

Model	Sequence Length	TP	PP	1F1B-I	ZB-V	Ours
12.1B LLM 16 GPUs	3072	4	4	41	30	53
		8	2	31	24	43
	6144	4	4	41	30	54
		8	2	31	24	43
26.3B LLM 32 GPUs	2048	4	8	55	38	72
		8	4	43	32	59
	4096	4	8	55	38	72
		8	4	43	32	59

Table 6: Experimental results on 12.1B and 26.3B LLMs in terms of throughput (samples per second). mbs represents the number of microbatches.

Model	Sequence Length	TP	PP	mbs	1F1B-I	ZB-V	Ours
12.1B LLM 16 GPUs	3072	4	4	64	9.52	9.12	9.87
				128	9.63	9.26	**10.1**
				192	9.66	9.31	**10.1**
		8	2	64	6.57	6.42	7.28
				128	6.60	6.46	7.32
				192	6.60	6.46	**7.33**
	6144	4	4	64	4.51	4.45	4.74
				128	4.57	4.48	4.82
				192	4.58	4.49	**4.83**
		8	2	64	3.11	3.13	3.46
				128	3.13	3.13	3.47
				192	3.11	3.13	**3.49**
26.3B LLM 32 GPUs	2048	4	8	96	12.3	12.4	13.0
				176	12.8	12.7	13.2
				256	12.7	12.8	**13.4**
		8	4	96	8.60	8.71	9.48
				176	8.67	8.79	9.56
				256	8.68	8.79	**9.61**
	4096	4	8	96	6.16	6.17	6.33
				176	6.17	6.28	6.49
				256	6.28	6.31	**6.51**
		8	4	96	4.23	4.26	4.66
				176	4.24	4.28	4.70
				256	4.25	4.29	**4.72**

D Comparison with Other Schedule Methods on H20 GPUs

We also conduct experiments on 16 NVIDIA H20 96G GPUs to evaluate the performance of our proposed schedule alongside other baselines, as summarized in Table 8. Our proposed schedule outperforms other approaches by a margin, but the performance improvement is far less significant compared to that achieved on A800 GPUs. This discrepancy can be primarily attributed to the characteristics of the H20 GPUs, which have lower BF16 FLOPs but higher communication

Table 7: Experimental results on 12.1B and 26.3B LLMs in terms of Model FLOPs Utilization (MFU, %).

Model	Sequence Length	TP	PP	mbs	1F1B-I	ZB-V	Ours
12.1B LLM 16 GPUs	3072	4	4	64	46.31	44.36	48.01
				128	46.84	45.04	**49.13**
				192	46.99	45.28	**49.13**
		8	2	64	31.96	31.23	35.41
				128	32.10	31.42	35.61
				192	32.10	31.42	**35.65**
	6144	4	4	64	50.16	49.50	52.72
				128	50.83	49.83	53.61
				192	50.94	49.94	**53.72**
		8	2	64	34.59	34.81	38.49
				128	34.81	34.81	38.60
				192	34.59	34.81	**38.82**
26.3B LLM 32 GPUs	2048	4	8	96	42.16	42.50	44.56
				176	43.87	43.53	45.24
				256	43.53	43.87	**45.93**
		8	4	96	29.48	29.85	32.49
				176	29.72	30.13	32.77
				256	29.75	30.13	**32.94**
	4096	4	8	96	46.32	46.40	47.60
				176	46.40	47.23	48.80
				256	47.23	47.45	**48.95**
		8	4	96	31.81	32.04	35.04
				176	31.88	32.19	35.34
				256	31.96	32.26	**35.49**

bandwidth. Furthermore, we profile the computation and communication times for the Attention and MLP modules of a single Transformer layer in the 12.1B Qwen2 model, as shown in Figure 13. It is evident that the proportion of TP communication is significantly lower than that measured on A800 GPUs. As a result, the benefits derived from optimizing TP bubbles have slightly diminished.

Table 8: Experimental results evaluated on 12.1B LLM on 16 H20 GPUs. mbs and seq_len denote the number of microbatches and the sequence length, respectively.

Configurations	TP	PP	Schedules	Throughput	MFU	Memory
mbs=192 seq_len=6144	2	8	1F1B-I	3.77	88.34	58
			ZB-V	3.63	85.06	**42**
			Ours	**3.79**	**88.81**	73
	4	4	1F1B-I	3.39	77.43	41
			ZB-V	3.30	77.32	**30**
			Ours	**3.44**	**80.61**	54
	8	2	1F1B-I	2.80	65.61	31
			ZB-V	2.80	65.61	**24**
			Ours	**2.89**	**67.72**	43

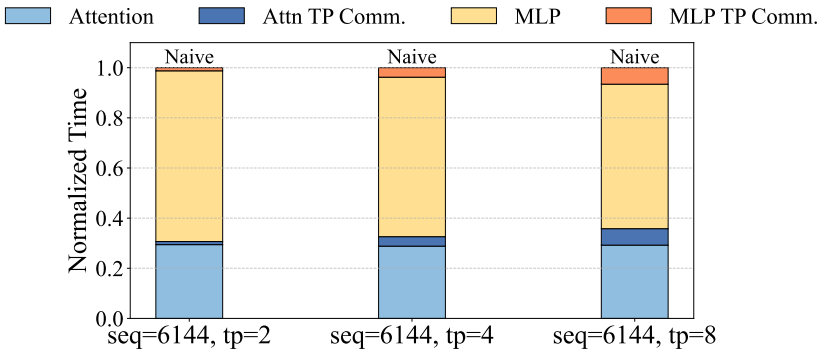

Figure 13: The computation and communication time proportion of Attention and MLP modules profiled on H20 GPUs.

E Evaluations with Existing Training Strategies

E.1 Activation Checkpointing

Our proposed schedule is compatible with activation checkpointing strategies. We conducted the experiment on Qwen2-12.1B using activation checkpointing (AC) with a batch size of 128 and a sequence length of 6k, and report the results in the following table:

Table 9: Performance comparison with different activation checkpointing configurations.

Config	Throughput (samples/s)	Peak Memory (GB)
AC disabled	4.79	56.0
AC enabled in Ours w/ MLP	4.19	44.7
AC enabled in Ours w/ Attn+MLP	3.94	41.5
AC enabled in Ours w/ Attn+MLP+Norm	3.75	36.3

As shown in Table 9, disabling AC yields the highest throughput of 4.79 samples per second but requires a peak memory footprint of 56.0 GB. Enabling AC selectively on the MLP modules reduces peak memory by 20.2% to 44.7 GB, with a corresponding throughput decrease of 12.5% to 4.19 samples/s. Extending AC to both Attention and MLP modules further reduces peak memory to 41.5 GB (a 25.9% reduction), while throughput declines to 3.94 samples/s. The most aggressive configuration, applying AC to all modules, achieves the greatest memory savings, reducing peak memory by 35.2% to 36.3 GB, at the cost of a 21.7% reduction in throughput, resulting in 3.75 samples/s. These results confirm that our scheduling framework is fully compatible with activation checkpointing strategies.

E.2 Data Parallelism and Context Parallelism

To demonstrate the compatibility of our schedule with both data parallelism (DP) and context parallelism (CP), we conduct experiments on a 12.1B Qwen2 model. As shown in Table 10, under identical tensor parallelism (TP=2) and pipeline parallelism (PP=4) configurations, our method achieves the highest throughput in both settings: 2.71 samples/s with CP (CP=2, $mbs = 128$, sequence length 12k) and 9.40 samples/s with DP (DP=2, $mbs = 256$, sequence length 4k). Our approach consistently outperforms baseline schedules (1F1B-I and ZB-V) across both parallelism paradigms, confirming its robustness and adaptability to different distributed training strategies.

F Impact of Communication Overlap on GEMM Execution Efficiency

In distributed training of large language models, overlapping communication (e.g., AllReduce) with computation (e.g., GEMM) is widely used to improve hardware utilization and reduce training time.

Table 10: Experimental results on 12.1B LLM compatible with data parallelism and context parallelism.

TP	PP	CP	mbs	Seq	Schedules	Throughput
2	4	2	128	12k	1F1B-I	2.64
					ZB-V	2.61
					Ours	**2.71**
TP	PP	DP	mbs	Seq	Schedules	Throughput
2	4	2	256	4k	1F1B-I	9.22
					ZB-V	9.16
					Ours	**9.40**

However, this overlap may cause resource contention, particularly for streaming multiprocessors (SMs) which potentially degrade GEMM performance.

To evaluate this effect, we conduct microbenchmarks under two scenarios: (1) GEMM dominates AllReduce, enabling full overlap; and (2) GEMM finishes early, leaving part of the communication exposed. In both cases, we compare overlapped execution against the sequential baseline (GEMM followed by AllReduce) and the standalone GEMM time.

Table 11: Execution times (in milliseconds) for GEMM, AllReduce, and their combinations under sequential and overlapped execution.

Operation	Experiment 1	Experiment 2
GEMM	8.605	0.334
AllReduce	3.364	1.643
GEMM + AllReduce (sequential)	11.969	1.977
GEMM with overlapped AllReduce	9.251	1.685

The results, summarized in Table 11, show that in the first scenario, where GEMM takes 8.605 ms and AllReduce 3.364 ms, the overlapped execution completes in 9.251 ms, only 7.5% slower than the GEMM alone and 22.6% faster than the sequential execution (11.969 ms). This indicates that the communication is effectively hidden with minimal interference.

In the second scenario, where GEMM is very short (0.334 ms) and AllReduce dominates (1.643 ms), the overlapped execution finishes in 1.685 ms, which is just 2.6% overhead over the AllReduce time and still 14.8% faster than the sequential baseline (1.977 ms). Notably, the GEMM itself is not measurably slowed down; rather, the slight increase in total time stems from the unavoidable tail of communication that cannot be hidden.